# TABLE OF CONTENTS VOLUME 2

## CHAPTER 1: INTRODUCTION
- Section 1.1 About Volume 2
- Section 1.2 A Look at How The Electronic Industry Got to Where It Is
- Section 1.3 The Boundary Between Low Speed and High Speed
- Section 1.4 When Does Crosstalk Become An Issue
- Section 1.5 Other Issues That High Speed Logic Circuits Create

## CHAPTER 2: THE PCB DESIGN PROCESS
- Section 2.1 Introduction
- Section 2.2 The Virtual Prototyping Process
- Section 2.3 Making The Conversion From Hardware Prototyping To Virtual Prototyping

## CHAPTER 3: POWER DELIVERY DETAILS
- Section 3.1 Introduction
- Section 3.2 Determining Load Currents and Their Variations
- Section 3.3 Things That Affect Power Supply Impedance
- Section 3.4 Function of Capacitors and Capacitance in Power Delivery System (PDS)
- Section 3.5 Calculating Capacitance Required to Achieve The Desired PDS Impedance
- Section 3.6 The Use of Ferrite Beads in Power Leads of Devices
- Section 3.7 Selecting Ceramic Capacitors
- Section 3.8 Determining The Parasitic Inductance of A DC to CD Converter or Capacitor
- Section 3.9 Plane Inductance
- Section 3.10 Signal Plane Fill
- Section 3.11 The Four Layer PCB Problem

## CHAPTER 4: PCB FABRICATION
- Section 4.1 Introduction
- Section 4.2 The Basic Multilayer Printed Circuit Board Fabrication Process
- Section 4.3 Blind and Buried Vias
- Section 4.4 Build Up Fabrication Process
- Section 4.5 Outer Layer Surface Finishes
- Section 4.6 Designing The PCB Stackup
- Section 4.7 Bare and Loaded Board Testing
- Section 4.8 Pad Stack Design and Drill Size Choices
- Section 4.9 Miscellaneous PCB Fabrication Topics

## CHAPTER 5: PCB MATERIALS
- Section 5.1 Introduction
- Section 5.2 Copper Foils
- Section 5.3 Glass Styles
- Section 5.4 Resin Types
- Section 5.5 Embedded Components

## CHAPTER 6: SIGNAL INTEGRITY AND PCB STRUCTURES
- Section 6.1 Split Planes
- Section 6.2 How Return Currents Find Their Way from Plane to Plane When a Signal Changes Layers
- Section 6.3 Determining The Size of Terminating Resistors
- Section 6.4 Maintaining The Integrity of Power and Ground

## Chapter 7: EMI AND EMC
- Section 7.1 What is EMI and Where Does It Comes From?
- Section 7.2 Understanding What EMI Is
- Section 7.3 What Makes A Good Antenna For Radiating EMI
- Section 7.4 Faraday Cages
- Section 7.5 A Discussion of Grounds
- Section 7.6 Getting Heat Out Of A Faraday Cage While Keeping EMI In
- Section 7.7 Getting Signals In And Out Of The Faraday Cage Without Letting EMI Out
- Section 7.8 Getting Power Into A Product Without Letting EMI Out
- Section 7.9 Building A Faraday Cage For A Rack Mounted Product With Plug In Cards and Backplane
- Section 7.10 Other Ways to Build A Faraday Cage
Figure 4.63. A PCB Showing Overlapping Clearance Holes in Planes................................................................. 90
Figure 4.64. A Plated Through Hole Shown in Cross Section.................................................................................. 90
Figure 4.65. A Top Down View of a Plated Through Hole in a PCB................................................................. 91
Figure 4.66. A Typical Thermal Tie in a Power Plane................................................................................................. 92
Figure 4.67. A Plane Layer Showing the Features of Interest.................................................................................. 93
Figure 4.68. A 0.5 mm Pitch BGA Fanned out to 1 mm Pitch............................................................................... 95
Figure 4.69. Drill Diameter vs. PCB Thickness and Aspect Ratio........................................................................... 96
Figure 4.70. Pad Stack Calculations for 10 mil TID and 2 mil Annular Ring.......................................................... 96
Figure 4.71. Pad Stack Calculations for 12 mil TID and 2 mil Annular Ring.......................................................... 97
Figure 4.72. Pad Stack Calculations for 10 mil TID and No Annular Ring............................................................. 97
Figure 4.73. Examples of Vias With and Without Back Drilling............................................................................ 99
Figure 4.74. A Data Path Operating at 5.2 GB/S........................................................................................................ 100
Figure 4.75. Loss vs. Frequency of the Signal Path Shown in Figure 4.74, With and Without Back Drilled Vias..... 100
Figure 4.76. A Quarter Wave Stub......................................................................................................................... 101
Figure 4.77. A Drill Chart Showing Drill Size by Hole Type.................................................................................... 102
Figure 4.78 A Set of Fabrication Notes for a High Speed Multilayer PCB Made from “Hi-Tg FR-4”............... 103
Figure 4.79. Typical PCB Fabrication Process Tolerances....................................................................................... 104
Figure 4.80. An Example of a Thermal Tie............................................................................................................... 105
Figure 4.81. Thermal Tie Illustrating Breakout........................................................................................................ 106
Figure 4.82. An Example of Wicking Along Glass Fibers......................................................................................... 108

CHAPTER 5:

Figure 5.1. Loss Tangent for Laminate Using “E” Glass vs. “S” Glass................................................................. 111
Table 5.1. Glass Styles Used in PCB Laminate....................................................................................................... 111
Figure 5.2. 106 Glass Cloth....................................................................................................................................... 112
Figure 5.3. 1080 Glass Cloth..................................................................................................................................... 112
Figure 5.4. 2113 Glass Cloth..................................................................................................................................... 112
Figure 5.5. 3313 Glass Cloth..................................................................................................................................... 112
Figure 5.6. 3070 Glass Cloth..................................................................................................................................... 112
Figure 5.7. 2116 Glass Cloth..................................................................................................................................... 112
Figure 5.8. 1652 Glass Cloth..................................................................................................................................... 112
Figure 5.9. 7628 Glass Cloth..................................................................................................................................... 112
Figure 5.10. TDR Test of a 50-Ohm Traveling Over 1080 Glass Cloth................................................................. 113
Figure 5.11. A Section Through a PCB Showing 3-Mil, 76 microns, Wide Traces with 106 and 7628 Glass Cloth... 114
Figure 5.12. A Cross Section View of Two Plies of 3313 Glass Weave............................................................... 114
Figure 5.13. TDR Test Results for Traces Routed over 3313 Glass Weave........................................................ 115
Table 5.2. Properties of Some Commonly Used Laminates..................................................................................... 116
Figure 5.14. Temperature Characteristics of Several Resin Systems................................................................. 117
Figure 5.15. An Inductor Formed in a Single PCB Layer......................................................................................... 119
Figure 5.16. Four Buried Resistors Used to Terminate ECL................................................................................ 120
Figure 5.17. Buried Resistors in a Vtt Plane of a Large PCB.................................................................................. 120

CHAPTER 6:

Figure 6.1. A Test PCB Containing Traces Which Cross Plane Cuts...................................................................... 124
Figure 6.2. A Transmission Line Passing Over a Power Plane Cut..................................................................... 124
Figure 6.3. A TDR Waveform of a Transmission Line Passing Over a Plane Cut............................................... 125
Figure 6.4. A Signal Changing Routing Layers and Reference Planes.............................................................. 126
Figure 6.5. Cross Section of a 18-Layer PCB in Figure 6.1.................................................................................... 127
Figure 6.6. Close up View of the Four Layer Changing Test Traces.................................................................. 127
Figure 6.7. TDR Plot of Test Trace With Layer Changing Via in the Center..................................................... 128
Figure 6.8. A 50-Ohm Transmission Line Showing Over and Under Termination and Perfect Termination in Z0.... 129
Figure 6.9. Waveforms on A Series Terminated Transmission Line................................................................... 130
Figure 6.10. Equivalent Circuit of a Series Terminated Transmission Line and Driver Circuit at T0.................. 130

CHAPTER 7:

Figure 7.1 Degradation to a 3.125 GB/S Output Signal as a Result of Inserting a Ferrite Bead in Its Power Lead.... 133
Figure 7.2. A Product With a Faraday Cage.......................................................................................................... 135
Figure 7.3. A Honey Comb Mesh Used to Contain EMI While Allowing Cooling Air to Pass.......................... 136
Figure 7.4 A 10Base2 Ethernet Circuit at The End of A Plug-In Card............................................................ 137
Figure 7.5. Emissions from a 10Base2 Shielded Cable Without an AC Connection Between Shield And Faraday Cage .................................................................................................................. 137
Figure 7.6. A Parallel Plate Capacitor Formed From the Copper Layers in the 4-Layer PCB......................... 138
CHAPTER 8:

Figure 8.1. A Typical LVDS Differential Logic Path.................................................................153
Figure 8.2. Current Flow In An LVDS Circuit for One Logic State........................................154
Figure 8.3. Current Flow In An LVDS Circuit For Opposite Logic State to Figure 8.3...........155
Figure 8.4. Differential Signal Waveforms Crossing..............................................................155
Figure 8.5. Side-by-Side Routing of a Differential Pair with a Noisy Line Routed Next to It....157
Figure 8.6. Geometry of Tightly Coupled and Loosely Coupled Differential Pairs.................158
Figure 8.7. Differential signal amplitude of 5-mil line/5-mil space, and 10-mil line/15-mil space differential pairs
Running at 2/4 GB/S over a 30'' long path.................................................................158
Figure 8.8. Potential Routing Problem With Tightly Spaced Differential Pairs......................159
Figure 8.9. Simulation Model of a 5.2 GB/S Data Path Containing 4 Meters of Infiniband Cable........160
Figure 8.10. Test PCBs Used to Measure Actual Path Losses...............................................161
Figure 8.11. Actual Measure Loss vs. Frequency Compared to Simulator Predictor Loss........162
Figure 8.12. Signal Leaving the Driver on the Left and Arriving at Receiver at 100 MB/S........162
Figure 8.13. Receiver Signal With Skin Effect and Dielectric Losses Removed and with Via Capacitance Removed.........................................................................................................163
Figure 8.14. Driver and Receiver Signals at 1 GB/S..............................................................164
Figure 8.15. Driver and Receiver Signals at 2.4 GB/S............................................................164
Figure 8.16. Receive Signal at 2.4 GB/S with Losses Removed (left) and Parasitic Capacitance Removed (right).....165
Figure 8.17. 2.4 GB/S Signal at Receiver with 2 pF Vi s Representing Backplane Connector Holes......165
Figure 8.18. Receiver Signal at 4.6 GB/S With Losses and Parasitics..................................165
Figure 8.19. 5.2 GB/S Signals Leaving Driver and Arriving at Receiver Without Pre-emphasis...166
Figure 8.20. 5.2 GB/S Signals Leaving Driver and Arriving at Receiver with 15% Pre-emphasis....166
Figure 8.21. Skin Effect Loss vs. Trace Width and Dielectric Loss for Three Laminates for a 33'' Path........168
Figure 8.22. A Parallel Terminated Net With Exact Matching and Mismatching.....................169
Figure 8.23. Loss vs. Frequency of Differential Paths With and Without Coupling Capacitors...170

CHAPTER 9:

Figure 9.1. A Virtual Prototyping Design Flow.................................................................171

CHAPTER 10:

Figure 10.1. Very Early IC Package (ECL Integrated Circuit In a Small Can)........................177
Figure 10.2. Dual-In-Line Package (DIP).............................................................................178
Figure 10.3. Amdahl 84-pin Quad Flat Pack (QFP)...............................................................178
Figure 10.4. EIT 2092-Ball HyperBGA Package.................................................................179
Figure 10.5. 1924 Pin Ceramic Column Grid Array.............................................................179
Figure 10.6. 10 Gb/s Line Card Block Diagram.................................................................181
Figure 10.7. Clock Xilinx Virtex2-Pro (Jitter = 1600ps).......................................................182
Figure 10.8. Data Bit-0 Eye Diagram Xilinx Virtex2-Pro......................................................182
Figure 10.9. Clock Xilinx Virtex-4 (Jitter = 97ps).................................................................182
Figure 10.10. Data Bit-0 Eye Diagram Xilinx Virtex-4........................................................182
Figure 10.11. Clock from IBM ASIC in a HyperBGA Package............................................182
Figure 10.12. Data Bit-0 Eye Diagram from IBM ASIC in a HyperBGA Package................182
Table 10.1. ASIC Clock Tree Current and Power Estimation..............................................185
Figure 10.13. ASIC Core Current and Voltage Waveforms...............................................186
Figure 10.14. Core Power Distribution Equivalent Circuit...............................................187
Table 10.2. Effective Frequency Range of Power Distribution Elements............................187