## THIRD IN A CONTINUING SERIES OF TEST LAB REPORTS.

AUTHOR: LEE RITCHEY, SPEEDING EDGE, APRIL 20, 2000

**WHAT EFFECT DO VIAS HAVE ON HIGH SPEED CIRCUITS?**

In the last Test Lab article I wrote titled "Examining Rules of Thumb", that was published in the January 2000 issue of PCD, I examined how cuts in power planes affect high speed signals and how solder mask affects the impedance of traces on surface layers. At the end of that article, I committed to address the issues surrounding the use of vias in the next article and here it is.

There are a variety of rules of thumbs in circulation concerning when to use vias, when they cannot be used, what effect they have on signals, etc. Further, do they look like inductors and/or do they look like capacitors?

Some relatively straightforward tests can be made to answer these questions. In addition, once we know just how vias appear electrically, we can include them in analytical models and simulate their effects.

There are two main uses for vias; as connections to power planes for bypass capacitors and component power leads and to allow us to enable layer changes when routing signals. The test results will help determine whether vias present problems in these areas and, if so, what characteristics are at work (parasitic inductance or capacitance), if any.

**Vias as Layer Changing Devices Look like Tiny Capacitors.**

From work done by earlier researchers (references 1 & 5 below), it has been established that vias behave like tiny capacitors when used to change layers on a signal trace. The questions are how big is this capacitor and will this capacitance have a detectable effect on a high-speed signal?

**Figure 1** is the layer 1 artwork for a test PCB done in 1998 to examine the capacitance value of 13 mil and 30 mil diameter vias in a 100 mil thick PCB. (Note: In reference #5 the capacitance value of a 40 mil diameter via 100 mils long was determined to be approximately 0.8 pF.) There are two arrays of traces running from left to right that contain varying numbers of vias. In each array there is a trace in the center with no vias. Above that trace are three traces, one with a via every 0.4 inch, one with a via every 0.2 inch and one with a via every 0.1 inch. These vias are drilled 13 mils in diameter. Below the center trace are three more traces like the first set, but with vias drilled 30 mils in diameter. The top array has traces on layer one, a surface microstrip layer, and the lower array has traces on layer four, a stripline layer.

The principle being exploited in this test is that adding capacitance along the length of a transmission line will lower its impedance. Using the equation: Zo = (Lo/Co)**.5, the square root of Lo/Co, where Co is the capacitance per unit length and Lo is the inductance per unit length of a transmission line, we can determine how much capacitance has been added in each case. All that is needed is to know the impedance of the trace with no vias and the impedance of the traces with vias**.** **Figure 2** is a set of TDR impedance measurements of four of the traces in the array. The top trace has no vias, the next trace has a via every 0.4 inches, the third trace has a via every 0.2 inches and the bottom trace has a via every 0.1 inches. Predictably, the impedance drops each time we add more vias (more capacitance).

From this data it is possible to use the impedance equation to calculate the capacitance of a single via. Table 1 shows the results of the calculations for both the 30 mil and the 13 mil vias. It can be seen that the average value for a 13 mil drilled diameter via 100 mils in length is approximately 0.27 pF and a 40 mil drilled diameter is approximately 0.66 pF.

If one calculates the outside area of the cylinder formed by each via, 13 mils, 30 mils and 40 mils, it can be seen that the capacitance is proportional to this area. This observation should allow the reader to apply these test results to other via diameters and lengths.

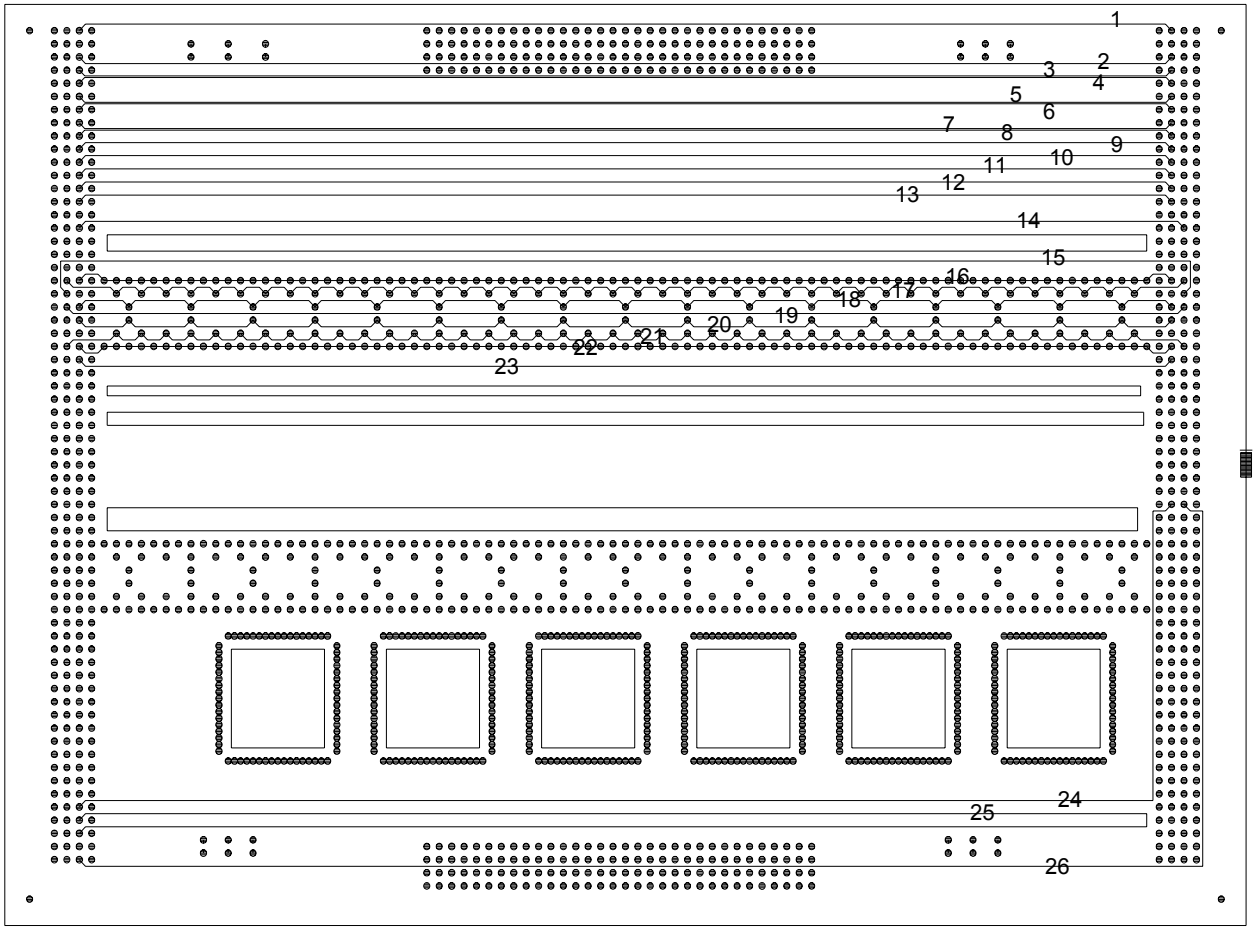
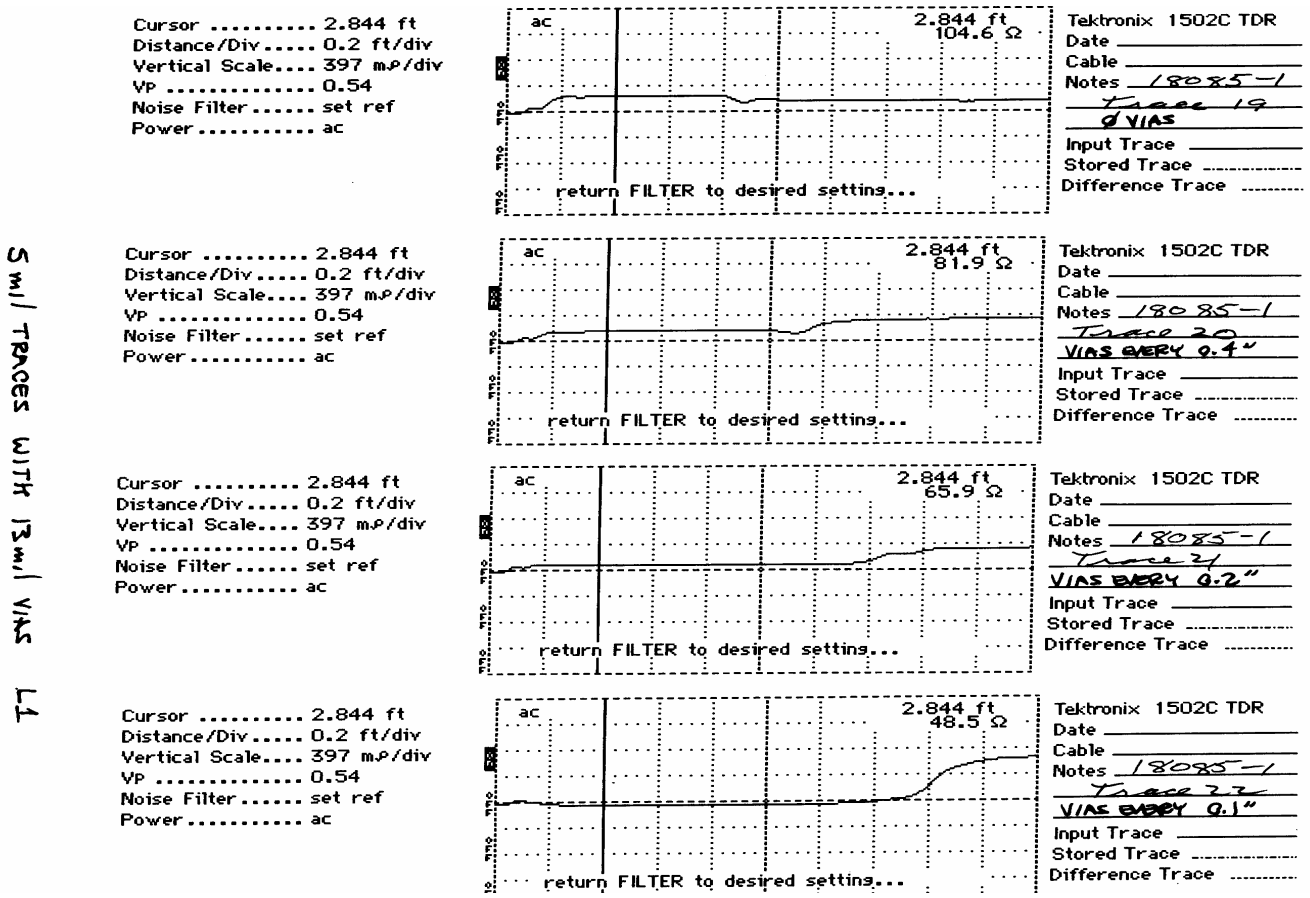



**Figure 1, Layer 1 Artwork of a Test PCB Showing Traces with vias added (Traces 16 to 22)**

The next question is whether this small capacitance will have a detectable effect on the quality of a high speed signal**. Figure 3** is a simulation of a 50 ohm BTL transmission line with a 0.3 pF via in the middle of it. There is a very small dip in the waveform (negative reflection) at the via site. To put this in perspective, **Figure 4** is a simulation of the same network with a single load added at the end of the transmission line. Notice how large the reflection is from the capacitance of the load compared to that from the via. The conclusion that can fairly be drawn from this set of tests is that small vias act like very small capacitors when used in a signal line. The effect of this very small capacitance is so small as to be of no consequence for edge rates as fast as 0.5 nanoseconds.




**Note how adding more vias (capacitance) increases electrical length and reduces impedance.**

## Figure 2, TDR Waveforms of Four Via Test Traces

| | | CALCULATION OF VIA CAPACITANCE BASED ON 14 LAYER TEST PCB | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |
| TRACE | Zo (ohms) | ZoxZo | Lo (nH) | Co(pF) | UNLOAD Co | C FROM VIA | VIAS/IN | C per VIA | VIA SIZE | AVE C |
| LAYER 1 | | | | pF | pF | pF | | pF | mils | pF |
| 15 | 32.5 | 1056 | 8 | 7.57 | 0.71 | 6.86 | 10 | 0.69 | 30 | |
| 16 | 49 | 2401 | 8 | 3.33 | 0.71 | 2.62 | 5 | 0.52 | 30 | 0.56 |
| 17 | 65.2 | 4251 | 8 | 1.88 | 0.71 | 1.17 | 2.5 | 0.47 | 30 | |
| 18 | 105.8 | 11194 | 8 | 0.71 | 0.71 | 0.00 | 0 | 0.00 | | |
| 19 | 82.3 | 6773 | 8 | 1.18 | 0.71 | 0.47 | 2.5 | 0.19 | 13 | |
| 20 | 66.1 | 4369 | 8 | 1.83 | 0.71 | 1.12 | 5 | 0.22 | 13 | 0.22 |
| 21 | 49.1 | 2411 | 8 | 3.32 | 0.71 | 2.60 | 10 | 0.26 | 13 | |
| LAYER 4 | | | | | | | | | | |
| 48 | 26.7 | 713 | 8 | 11.22 | 2.44 | 8.79 | 10 | 0.88 | 30 | |
| 49 | 35.8 | 1282 | 8 | 6.24 | 2.44 | 3.81 | 5 | 0.76 | 30 | 0.76 |
| 50 | 44.7 | 1998 | 8 | 4.00 | 2.44 | 1.57 | 2.5 | 0.63 | 30 | |
| 51 | 57.3 | 3283 | 8 | 2.44 | 2.44 | 0.00 | 0 | 0.00 | | |
| 52 | 50.3 | 2530 | 8 | 3.16 | 2.44 | 0.73 | 2.5 | 0.29 | 13 | |
| 53 | 44 | 1936 | 8 | 4.13 | 2.44 | 1.70 | 5 | 0.34 | 13 | 0.32 |
| 54 | 37.1 | 1376 | 8 | 5.81 | 2.44 | 3.38 | 10 | 0.34 | 13 | |
| | | | | | | | | | | |
| APRIL 1998 | | PREPARED BY LEE W. RITCHEY | | | | | | | | |

**Vias are capacitive, not inductive when used to change layers. The capacitance value of a via is small compared to the capacitance of a trace (3.5pF/inch for 50 ohms). In general, vias are not visible to signals with edge rates slower than .3 nSEC.**

## Table 1, Results of Via Tests

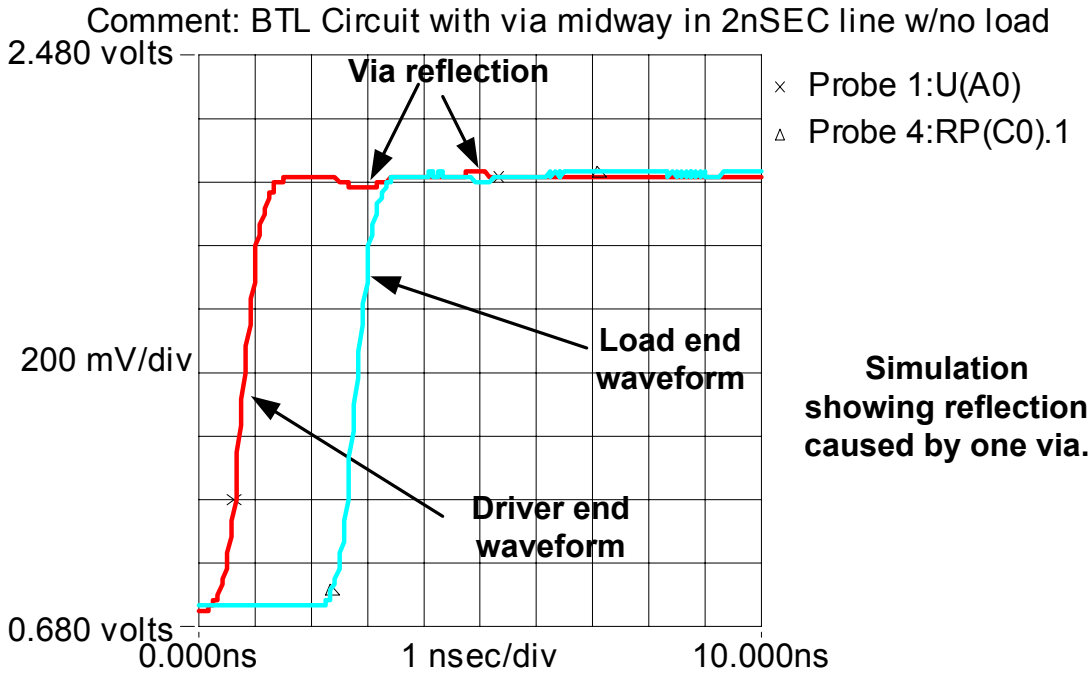



**Figure 4, Simulation of a 0.3 pF Via in the middle of a 12 inch long 50 Ohm Transmission Line**

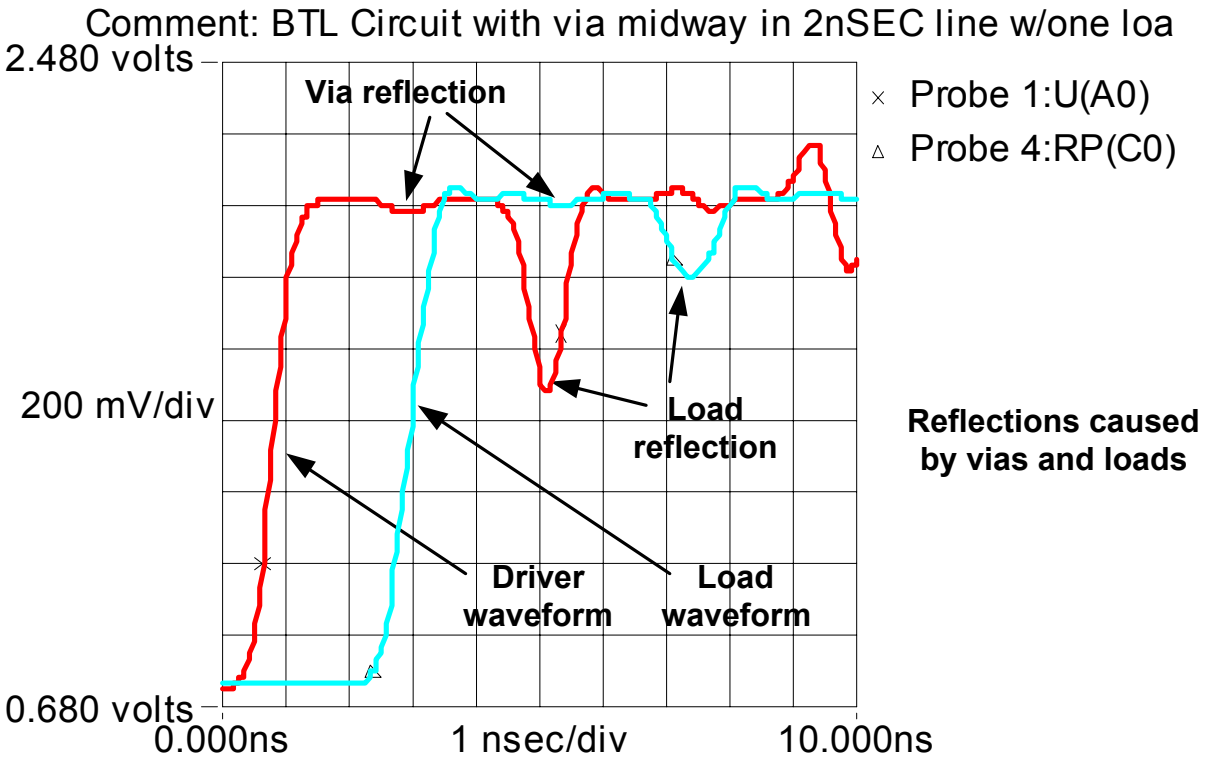
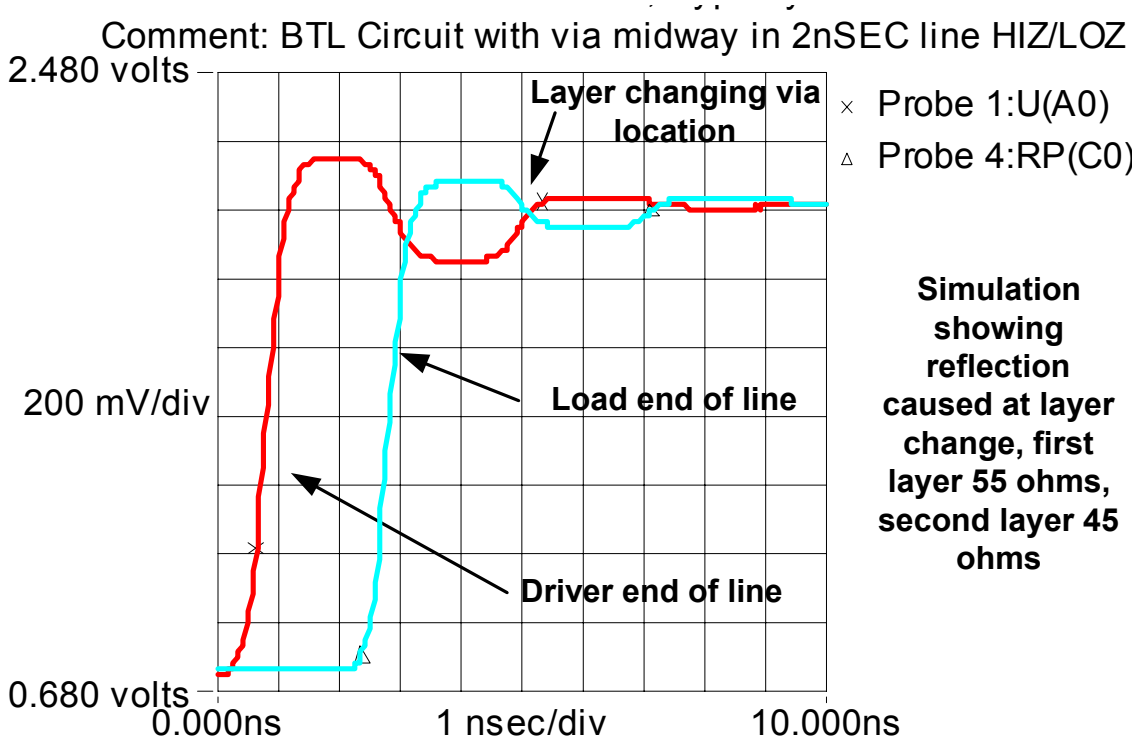



**Figure 4, Simulation of a 0.3 pF Via in the middle of a 12 inch long 50 Ohm Transmission Line with one BTL Load at the End.**

**Vias as layer Changing Devices When the Impedances are Different in Two Layers Being Used**

From the previous analysis it can be seen that there is no detectable reflection caused by a via when it is used to change layers when the impedance of the two layers is the same. In production, controlled impedance PCBs can have impedance variations of as much as 10% around their nominal values. In the case where one layer is +10% and the other is -10%, changing layers with a via will result in a reflection like that shown in Figure 5. This simulation depicts a 50 ohm transmission line with just such a variation in impedance. This is typical of the degree of mismatch that occurs in real designs and must be accounted for when creating design rules. The author believes that this reflection is often attributed to the via, rather than to the two different impedances, giving vias the undeserved reputation that they cause reflections.




## Vias Used to Connect Power Leads to Planes Look Like small Inductors.

Many tests have been made to determine the inductive value of vias. In Reference 2, Power Bus Decoupling on Multilayer Printed Circuit Boards, the authors build a variety of via structures to connect surface mount capacitors to the power planes, ranging from five vias in pad to one via per pad tangent to the pad. The one via tangent to pad solution is the most common connection method. This structure, two vias and two pads, resulted in a 2 nanohenry total inductance, or less than 1 nanohenry for a single via.

In order to decide whether this unwanted parasitic inductance is acceptable or not, the circuit using the vias must be analyzed to determine how much power system degradation they create. Once this is known, a determination can be made about the acceptability of the connection.

**Conclusion**

Vias have both parasitic inductance and parasitic capacitance. When vias are used as layer changing devices, the parasitic capacitance is visible. When vias are used to connect to power planes, the parasitic inductance is visible.

In the layer changing case, the impact of the via on signal quality is negligible. As a result, designers need not worry about the use of vias having an adverse effect on signal quality. True, the impedance mismatches when changing layers is significant. One could argue that barring the use of vias makes this problem go away. Unfortunately, this is not the case. This same amount of mismatch will occur where the traces meet terminations and where signals change from one PCB to another. Because of this, the design rules will need to be robust enough to allow for these unavoidable mismatches. Once this has been done, the use of vias will have been accounted for and there will be no benefit in restricting their use.

In the case where vias are used to make connections to the power planes, the parasitic inductance will be visible. The power leads of all IC packages, other than well designed BGA packages, will be 4 nanohenries or more, significantly larger than the via inductance. If the unwanted power connection degradation is excessive, the package lead frame will constitute a problem long before the via will.

References:

1. SPICE modeling of circuit effects extraction for high bandwidth PWB design, Smith, Joseph, etal, IPC Technical Review, November 1966. Contains SPICE model of a via predicting inductance and capacitance.

2. Power Bus Decoupling on Multilayer Printed Circuit Boards, Hubing, etal, IEEE Transactions on Electromagnetic Compatibility, Vol. 37, No 2, May 1995. Good via inductance tests.

3. 90 Degree Corners, The Final Turn, Brooks, Doug, Printed Circuit Design, January 1998. This is the first test lab article.

4. Examining Rules of Thumb, Ritchey, Lee W. Printed Circuit Design, January 2000.

5. A Test PCB to Evaluate Effects of various PCB Structures on Transmission Lines, Ritchey, Lee W, etal, Nepcon Proceedings, Spring 1989.