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Intelligent Design

Managing the Tradeoff Between PCB Cost and Signal Quality at 10 Gigabits per Second Data Rates

In my April column, I covered how the choice of glass weave can influence the amount of jitter that is added to a high data rate signal by the PCB itself. In this column I will examine how the method used to route a 10 gigabit per second data signal can affect quality.

It is well known that the parasitic capacitance of the vias used to connect signals from integrated circuit and connector pins to traces in PCBs can adversely affect signal quality. As the data rate increases, this parasitic capacitance often is the limiting factor on how high the data rate can be driven in a conventional PCB.

At data rates of 10 gigabits per second, the capacitance of these plated through holes or vias is the primary factor limiting performance. One way to avoid this limitation is to route the entire signal trace on the top layer of the PCB connecting two IC pins without the use of vias or plated through holes. This is the most common technique currently in use for connections between the transceivers which connect the logic devices and fiber optic cables. This method is doing a reasonable job. However, it has several drawbacks.

The first of these drawbacks is that the impedance of traces on outer layers of PCBs is more difficult to control because of plating and etching irregularities and variations in the thickness of the prepreg that separates the surface layer from the underlying plane.

The second of these is that the most common surface finishes for PCBs that contain these traces is either electroplated gold over electroplated nickel or ENIG, both of which contain significant amounts of nickel. Nickel is a ferromagnetic metal. Ferromagnetic metals react with the electromagnetic fields in these very fast signals in such a way that the signal loss is much higher than might be expected from an ordinary copper trace.

The third of these is that space on the outer layers for signals is often blocked by the mounting pads of the components themselves limiting the number of signals that can actually be routed on the top layer of the PCB. Users trying to connect multiple rows of serdes (logic devices) to transceivers find it difficult, if not impossible, to make all of the connections on the top layer.

Figure 1 shows a method for solving the above problems. Instead of routing these signals on the top layer, laser drilled, blind vias are used to access layer 2 on which the signal traces are routed. This provides several benefits. The traces are etched on an inner layer where width and thickness control are more precise than on the outer layer. The primary dimension affecting impedance after trace width is the spacing to the nearest plane. In this case, the dielectric forming this dimension is laminate that can be selected with a well-controlled thickness in advance of lamination. Since the traces are not on the top layer, they are not plated with nickel, so the ferromagnetic losses are avoided.

Since the traces are not on the top layer, it is possible to route more of them between serdes and the transceivers, solving the congestion problem associated with multiple rows of transceivers on a PCB such as a switch or router product, with a high number of ports.

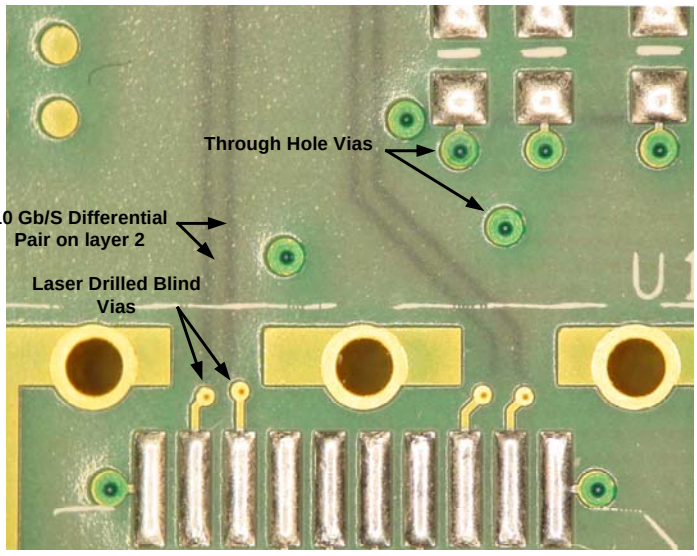

Figure 1. Laser Drilled Blind Vias

The only penalty associated with using this method is the need to add a laser drilling step to the process. It should be noted that the blind vias are not drilled in the mounting pads of the devices. Instead, short "dog bones" are added and the blind vias are drilled in a small pad outside the device mounting pads. The reason for doing this is to avoid trapping a small gas bubble under the ball when soldering is done. (This is known to weaken the solder connection to a BGA ball.)

10 gigabit per second data rates do indeed push the envelope of traditional PCB implementations. And, successfully managing the development of these PCBs can be a costly undertaking. But, it is possible to design and manufacture reliable, cost-effective boards if careful attention is paid to some of the "basics" such as glass weave selection, laminate thickness, via drilling and signal routing.