FAQ #5

For Current Source Newsletter #7

Why Not Route Two Traces Between Pins on a 1 mm Pitch BGA?

There are applications notes that describe how to save layers in a PCB by routing two traces between pins on a 1 mm pitch BGA. This practice has been recommended by one of the leading FPGA vendors as a way to use their very high pin count FPGAs in a low layer count PCB. When this approach is used with a high layer count PCB the result is often, if not always, a PCB that has very poor yields and is unreliable when it is used in a system under actual conditions as opposed to a laboratory or a prototype built in a small volume by a specialty shop. The following discussion will illustrate why this approach results in unsatisfactory yields when volume manufacture is attempted with this approach.

A Look at the Geometry Associated With Plated Through Holes in a PCB

To understand the space that can be used to route traces in signal layers of a multilayer PCB, (this also applies to four layer PCBs) it is useful to look at how plated through holes (vias) are created and the various requirements that must be met by the finished PCB. Figure 1 is a section through a plated through hole showing signal and plane layers.

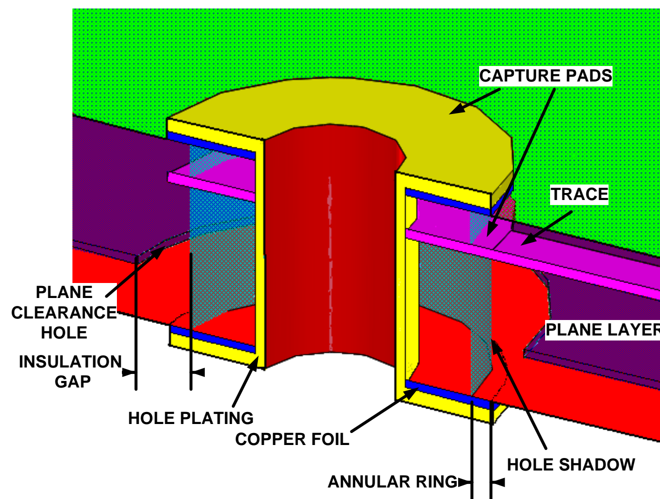

Figure 1 A Section Through a Plated Through Hole in a PCB

Deciding on the dimensions of the features in this diagram is often called pad stack design. (This subject is discussed at length in Volume 2 of RTFTAPHHSD). The elements in a pad stack design are the size of the finished hole, the size of the drilled hole, the size of the capture pad in a signal or surface layer used to connect to traces and component leads and the size of the clearance hole or antipad in the plane layers. Things that must be accounted for are minimum thickness of copper plating in the hole, allowance for drill wander in the fabrication process, allowance for misregistration between layers of the PCB, minimum insulation thickness between plating in the hole and metal in the signal and plane layers and adequate copper bonding between traces and the plating in the hole.

As will be seen, the dimensioning involved in designing pad stacks is done from the edges of the drilled, plated hole to features inside the PCB or the drill size. Traditionally, the PCB design process has begun with the diameter of the finished, plated through hole. The choice of drill size has been left to the individual PCB fabricator and the size of clearance holes and capture pads in signal layers has been made large enough that there was ample room for a wide range of drill sizes. As the pitch between device pins has shrunk over the years, this practice has resulted in PCBs with poor manufacturing yields.

To solve this problem, it has become necessary for the designer of the PCB pad stacks to take charge of specifying the drill size as well as the finished hole size. To get from finished hole size to drill size one only need to take the finished hole size and add 4 mils (.102 mm) to the finished hole size. Then, designing the pad stack can proceed from the drill size. (Once these dimensions are chosen the drill size must not be changed. If the drill size is made smaller than that specified the aspect ratio may grow too large and plating may not be completed all the way through the hole. If the drill size is made too large, the clearances to copper in adjacent layers may be too small or the drill may break out the side of the capture pad on a signal layer.)

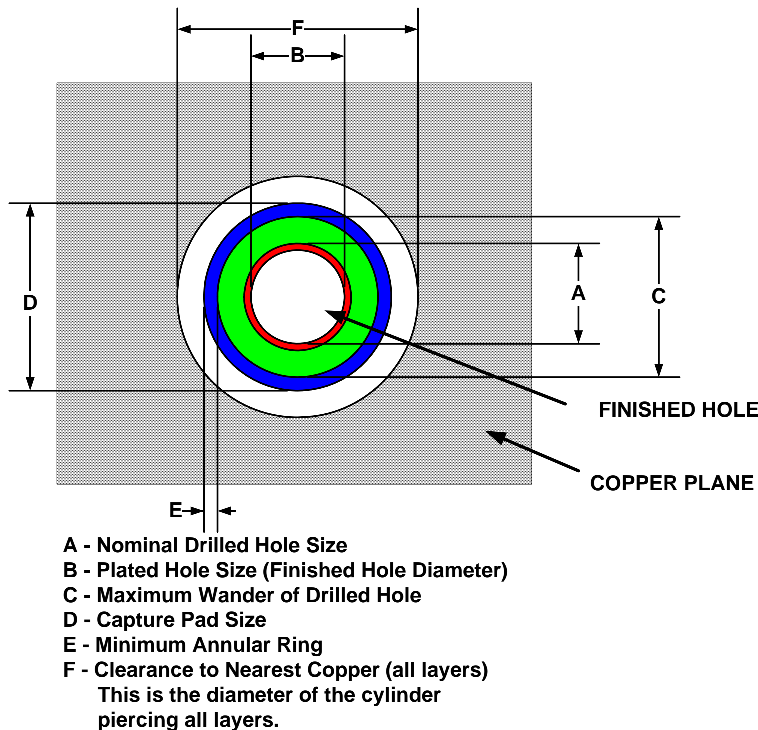

Figure 2. A Top Down View of a Plated Through Hole

Figure 2 is a top down view of a plated through hole or via showing the clearance hole or pad in a power plane of diameter F. This is the minimum opening in the power planes needed to guarantee that there is enough room for the drilled hole, the drill wander and minimum insulation to nearest copper in any layer, be it signal or power. In Figure 3 an array of vias or holes spaced on a 1 mm pitch is shown. The web between clearance pads is what is available for traces on signal layers and for copper in the plane layers to conduct the current used by the ICs and other devices on the PCB. (It should be noted that if the trace width were the same as the web in the plane, the impedance of the trace would raise several ohms as it passes over the array of holes under a BGA. To minimize this effect, the web should be wider than the trace by about 2:1.)

Calculating Width of Plane Webs and Routing Channels in Signal Layers

Clearly, the width of a plane web is the hole pitch minus the diameter of the clearance pad or hole. The question is how to arrive at the diameter of the clearance hole needed to satisfy all of the constraints. These constraints are: drilled hole large enough to insure proper plating; room around the drilled hole to allow for drill wander and minimum insulation thickness.

Minimum Drilled Hole Size

Determining the minimum drill size needed to insure proper copper plating requires knowledge of the maximum aspect ratio of the drilled hole. Aspect ratio is defined as the ratio of hole length to diameter. This is covered in detail in Chapter 4 of Volume 2. For now, the maximum aspect ratio for the top fabricators in the world is 10:1 for volume production. For the mid tier fabricators it is 8:1 and for the low-end fabricators it is 6:1. Of course, the minimum drill size is also influenced by the thickness of the PCB. For example, if the PCB is 120 mils thick and is being built by a top-tier fabricator the minimum drill size would be 12 mils. For a mid-tier fabricator it would be 15 mils and for a low-end fabricator it would be 20 mils. (As will be seen from the following analysis, with component lead pitches of 1 mm or more, a 12-mil drill works well. For this reason, this is my default smallest drill size even if the PCB thickness is less than 120 mils.)

Most of the high performance PCBs being designed today are often 120 mils thick. This analysis will be for such a PCB built by a top-tier fabricator.

Allowance for Hole Wander

Drilled holes are often not exactly where they were designed to be. There are a number of reasons for this. Among these are: ability of the drill machine to locate the exact spot where the hole is to be drilled; shrinkage of the layers of the PCB during lamination; dimensional errors in the film used to image the layers of the PCB; and misregistration of the layers during lamination. All of these errors add up to a position error for the drill that is often referred to as TIR (total included radius) of

TID (total included diameter). The top-tier fabricators can hold a TIR of 5 mils (TID of 10 mils) across an 18” x 24” panel- the most commonly used panel size.

Therefore, we must allow 5 mils per side of the drilled hole for drill wander. This produces what I call a hole shadow that the drilled hole casts all the way through the PCB. This shadow defines where we might find copper that is connected to the via or trace. We must keep away from this shadow in all layers by a distance that is defined by the insulation requirement for the PCB.

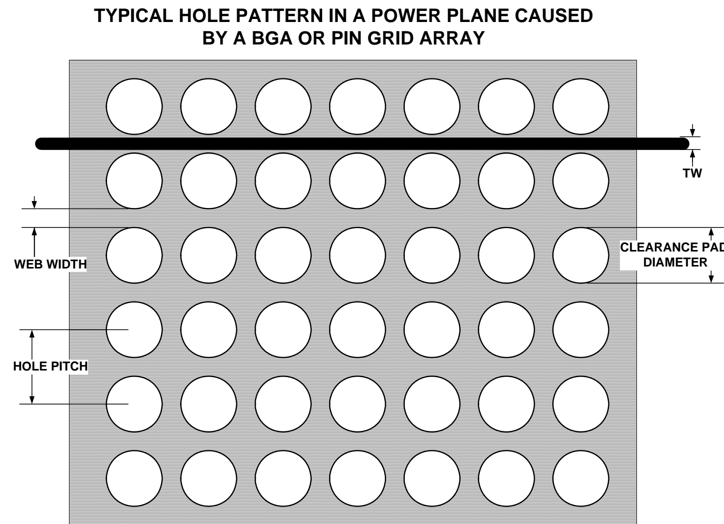

Figure 3. A View of a Plane With a Trace Traveling Over It

Minimum Insulation Requirement

Most laminate has a breakdown voltage on the order of 1000 volts per mil of thickness. Many systems require a minimum breakdown voltage or hipot test of at least 500 volts and most Internet or Telco products require 2000 volts. Being conservative, it is good to design for the more difficult requirement or 2000 Volts. This would require a minimum of 2 mils of dielectric between opposing circuits or between traces or planes and the plating in the hole. This would require the clearance hole diameter to be 4 mils larger in diameter than the hole shadow.

The problem with this small dimension is that it does not account for the fact that the chemistry involved in etching, cleaning and plating will wick along the glass fibers in the weave of the laminate layers. Figure 4 is a section through a plated through hole showing wicking along the glass fibers. To lend some scale to the photo, the copper layers are 0.5 mils thick. Some of the wicking is as much as six times this or 3 mils. This wicking is conductive. Therefore, it effectively increases the diameter of the plated though hole by this amount per side or 6 mils total.

Adding the 2 mils per side required for insulation and 3 mils per side for wicking the total insulation thickness required to meet the insulation requirement is 5 mils per side.

Adding it All Up

Using the above information, it is possible to determine the plane web available for conducting current and space available for routing traces between pins of a 1 mm pitch BGA. For the 120 mil thick PCB, the minimum drill size is 12 mils. Referring to Figure 2, the diameter of the finished hole size would be 4 mils less than this or 8 mils nominal. The hole shadow would be the 12-mil drill plus 10 mils for hole wander or 22 mils. The clearance hole in a plane would be 22 mils plus 10 mils for insulation allowance or 32 mils.

The hole-to-hole distance of a 1mm pitch BGA is 39.37 mils. Subtracting 32 mils from this results in a web width or trace routing channel width of 7.37 mils. This is ample room for a 5 or 6 mil trace. If one attempted to route two traces between holes (assume they are 3 mil traces with a 4 mils space) the total width required would be 10 mils. Clearly, one of the requirements spelled out above would be violated and the PCB would suffer from yield problems.

Preventing Breakout of Capture Pads on Signal Layers

The connection between a trace and a plated through hole is made by flashing a pad on the signal layer that is connected edge on to the plating in the hole. This can be seen in Figure 4 on the second layer from the top. The size of this pad has a direct relationship to overall reliability of the assembled PCB. If the contact between the trace and the plating in the hole is just the cross section of the trace, a **butt connection**, this bond is not strong and is likely to be broken during soldering or

rework resulting in an intermittent PCB. The solution to this problem is to make the capture pads on the signal layers larger than the hole shadow by enough to guarantee no butt connections ever occur no matter where the drilled hole lands within the shadow. This allowance is called an **annular ring**. Depending on the reliability level required of a product the annular ring may be 1 mil or 2 mils or 0 mils.

Products that are intended for the consumer market have a lower reliability requirement than those destined for computers, military equipment or the Telco markets. In the latter case, the minimum annular ring for a capture pad in a signal layer is 1 mil. This means that these capture pads must be larger than the hole shadow by 2 mils. In the above analysis, the hole shadow was calculated to be 22 mils. This would require a capture pad of 24-mil diameter.

When the insulation requirement of 5 mils per side is added to this, the result is 34 mils. Subtracting this from the 39.37 mil pitch of the BGA one arrives at a useful space for traces of only 5.37 mils. Clearly, there isn't even room for a 6 mil trace much less two traces!

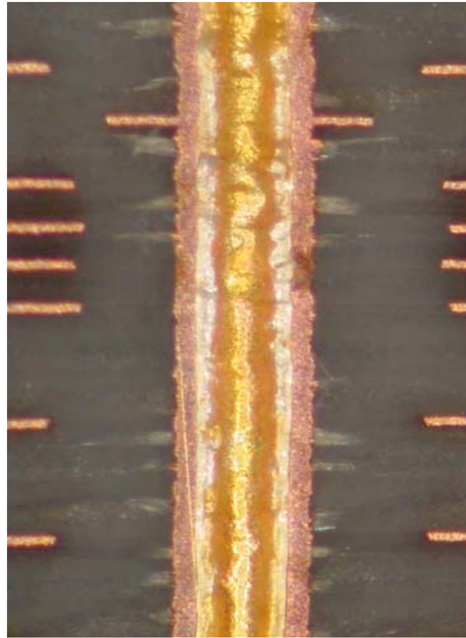

Figure 4. A Section Through A Plated Through Hole Showing Wicking Along Glass Fibers

Conclusions

All of the features associated with a drilled hole in all of the layers are commonly called a pad stack. In this example the pad stack is as follows:

Drill size-	12 mils
Finished hole size-	8 mils nominal
Capture pad size-	24 mils
Annular ring-	1 mil
Clearance hole-	32 mils
Web with for 1mm pitch-	7.37 mils
Maximum trace width-	5.37 mils

In order to preserve routing space throughout the signal layers, the minimum pitch of routing vias or component holes for surface mount parts is `1 mm. Any via or hole for connecting a lead of a surface mount part to an internal layer should use this pad stack.

All other plated through holes should have their pad stacks designed as follows:

Drill size = finished hole size + 4 mils
Capture pad size = drilled hole size + 12 mils
Clearance hole size = drilled hole size + 20 mils

Minimum hole pitch = (d1 + d2) +20 mils + minimum web requirement (usually no less than 7 mils).

Some Observations

From the above it can be seen that routing two traces between pins of a 1 mm pitch BGA will result in a low yielding and unreliable PCB. Once it is agreed that it is only possible to route one trace between pins, as long as the trace width is 5 mils or less, it is possible to specify a minimum drill size of 12 mils. There is no good reason to specify a smaller drill size and the difficulties that it would entail- especially potentially unreliable plating.

If one is fortunate to have access to 50-mil pitch (1.27 mm) BGAs, the space available for traces is 50 mils less 32 mils or 18 mils. This is plenty of room for two traces between pins and the space needed to separate them. Any time there is a choice between a 1mm pitch component and a 50-mil pitch component, the choice is clear. IC manufacturers would do their customers a great service to stick with 50-mil pitch BGAs when the pin count is high. They do their customers a grave disservice when they specify 0.8 mm pitch components as will be seen in a later FAQ.

References:

1. Right the First Time, A Practical Handbook on High Speed PCB and System Design, Volume 2, Chapter4 and Appendices 6, 7 and 10.