10 layer PCB stackup 165
2 Via footprint 142
2D field solvers 84, 89
4 Via footprints 142
6 Via footprints 143
A/D 45
AC ground 43
AC termination 64
Aluminum electrolytic capacitor 132
Amplitude, current spike 153
Analog and video circuits 32
Analog ground 45
Annular ring 262
Applications notes 17
Aspect ratio 211, 272
Assembly drawing 226
Assembly files 226
Asymmetrical stripline 83
Backplane buses, parallel 74
Backplane buses, series 74
Backward crosstalk 103
Bad BGA packages 181
Bench voltage 53
Bismalimine triazine 201
Blind via limitations 212
Blind vias 211
BT 201
BTL 100
Building up 272
Buried microstrip 209
Buried micro-stripline 83
Buried resistors 74
Buried vias 212
Bus protocols 99
Bus transistor logic 100
Bypass capacitors 40
CAD net list 274
CAM/Gerber data checkers 218
Cap layer lamination 271
Cap layers 208
Capacitance 39
Capacitance, parallel plate 144
Capacitive coupling 103
Capacitive crosstalk 103
Capacitive reactance 39
Capacitor arrays 132
Capacitor characterization 134
Capacitor equivalent circuit 133
Capacitor placement 147
Capacitor via length 143
Capture pad 262
Ceramic capacitor 132
Chassis ground 45
Circuit complexity 18
Circuit element sizes 19
Clearance hole 262
Common mode coupling 115
Compliance window 116
Concept of ground 45
Controlled depth drilling 211
Controlling the impedance 29
Copper foil 262
Cost vs. price 15
Coulomb 39
Coupling capacitors 40
Coupling 103
Creating a stackup 209
Critical length 34, 105
Crossing detector 116
Crosstalk 103
Crow fly length 223
Current flow and voltage drop 30
Current sources 96
Current spike amplitude 153
Current steering 116
Current switch 116
Cyanate ester 201
Data base management 18
DC voltage drop 127
DC-Dc converter 124
DDR-1 122
DDR-2 122
DDR-SDRAM interface 160
DDR-SDRAM power 162
DDR-SDRAM Vtt 167
Dead time 62, 71
Decoupling capacitors for 2.5V 165
Decoupling capacitors 40, 132
Design files 228
Design rule checking 270
Details 196
Detour routing 223
Dielectric breakdown voltage 205
Dielectric constant 19
Dielectric loss 19, 120
Differential impedance 120
Differential signaling 114
Digital circuits 32
Digital ground 45
Diode termination 64
Directional couplers 105
Documentation 226
Dog box 267
Down time 69
Drilled hole size 262
Drilling 197, 272
Driver types 96
DVT 214
ECL 100
Edge rate 33
Einstein, Albert 16
Electroless nickel and gold 273
Electroless plating 273
Electroless silver 274
Electroless tin 273
Electrolytic plating 273
Electromagnetic fields 26, 30
Electronic taping 221
Electroplated copper 273
Electroplated gold over nickel 273
Electroplated palladium 273
Electroplated tin 273
Electroplated tin/lead 273
EM fields 31
Emitter coupled logic 100
Emitter coupled pair 116
Engineering drawing 226
ENIG 273

EPC 36
Equivalent parallel capacitance 36
Equivalent series inductance 40
Equivalent series resistance 36, 40
Er 33
ESL vs. via length 143
ESL 40, 133
ESR 36, 40, 133
Etched pairs 196
Etching outer layers 197
f 36
Fabrication drawing 226
Fan out clock buffers 73
Farad 39
Farad, Michael 39
Faraday cages 45, 46
Feature accuracy 19
Fiber channel 120
Finished hole size 262
Floor planning tools 216
Foil Lamination 196, 271
Forced sequencing 76
Forward crosstalk 103
Fourier transform 78
F_r 40
FR-4 201
Frequency-Amplitude table 136
Fringing capacitance 85
GETEK™ 201
Glass to resin ratio 81
Glass transition temperature 201, 202
Golden board testing 274
Ground bounce 176
Ground bounce tests 178
Ground bounce 117
Ground offsets 188
Ground offsets 114
Ground traces 108
Ground 43
GTL bus 100
Guard traces 108
Gunning transistor logic 100
Gunning, Bill 100
Harmonic 86
Heavy use power 155
Henry 36
Henry, Joseph 36
High Speeding 59
HIPOT 267
Hole plating 262
Hole shadow 262
HSTL bus capacitive loading 158
HSTL bus termination 155
HSTL waveform 158
Hyper-transport 120
I/O peak current 155
IBIS models 217
Ideal capacitor 40
Ideal component data sheet 229
Ideal inductor 37
Ideal resistor 41
Ideal voltage source 96
Impedance equation 47
Impedance matching 18
Impedance test trace 199
Impedance 36, 47
Inductance, circular plate 146
Inductance, power plane 144
Inductive crosstalk 103
Inductive reactance 36
Inductor 37
Inner layer etching 197
Insulation gap 262
Interplane capacitance 207
Isola corporation 204
L 36
Laminate materials 268
Lamination 197, 270
Laser drilling 211
Layer count 19
Library maintenance 216
Load types 98
Loads 21
Logic emulators 217
Logic simulation tools 217
Loss tangent 204
Loss tangent vs. PCB cost 205
Low ESR Tantalum capacitor 132
Low speed 59
Low voltage differential signaling 101
L_P 124
LVDS bus termination 159
LVDS 101
Magnetic coupling 103
Manhattan length 223
Manufacturing tolerance 262
Martin Marietta 108
Mass lamination 271
Matched impedance drivers 97
Materials engineering 268
Maximum allowable logic 0 57
Maximum allowable logic 1 57
Maximum power 155
Maze based routing 221
Mechanical transmission lines 26
Merix corporation 204
Micro BGA 213
Micro-stripline 44, 83
Microvia 211
Minimum allowable logic 0 57
Minimum allowable logic 1 57
Nanohenry 36
Nanosecond 33
Net 223
Net list compare 274
Noise margin analysis 192
Noise margins 183
Noise sources 184
Ohm 41
Ohm, George Simon 41
Ohm's Law 41
OSP 274
Overshoot 51
Package inductance 177, 180
Pad stack 262
Pad stack calculations 262
Panel sizes 270
Parallel plate capacitance 85, 144

Parallel resonance 134
Parallel terminated TL 71
Parallel termination 28, 63
Parallel tuned circuit 36
Parasitic capacitance 37, 98
Parasitic inductance 37
Parasitic resistance 37
PCB fabrication 196
PCB routers 218
PCB routing 221
PCB Stackup 125
PCI bus 99
PCI Express 120
Peak current 155
Photo-imaged vias 212
Picofarad 39
Picoseconds 33
Plane 262
Plane capacitance 170
Plane fill 172
Plane resonance 149
Plating outer layers 197
Pocket knife engineering 214
Polyimide 201
Possible vs. reasonable 16
Power dissipation 152
Power dissipation 152
Power distribution drop 128
Power plane capacitance 139
Power plane inductance 124, 144
Power plane resistance 124
Power planes 46
Power sources 21
Power subsystem design 186
Power subsystem 122
Power Supply variance 192
Power system simulators 218
Power system tests 175
Prepreg 196
Press cycle 197
Process tolerances 205
Propagation velocity 149
Quarter wave stubs 78
Rambus 102
Rats nest 221, 223
Real capacitor 40
Real inductor 37
Real parts 24
Real resistor 41
Real voltage sources 96
Reference accuracy 190
Reflected wave switching 29, 62
Reflection equation 50, 80
Reflection 28
Reflections 50, 187
Registration 271
Relative dielectric constant 203
Relative dielectric constant 33, 49
Remote sense 128
Resin content 203
Resistance 41
Resonance, parallel planes 149
RF and microwave circuits 32
Right angle bends 90
Ring back 51
Ringing 53
Rise and fall time 33
Round trip delay 62
Routing via 92, 223
R_P 124
R-packs 191
Rule sets 16
Rules of thumb 15
Ruskin, John 15
Scheduling 76
Schematic capture tools 216
Segment 223
Self resonant frequency 38
Sequencing 76
Sequential blind vias 212
Sequential lamination 271
Series resonance 133
Series resonant circuit 40
Series stub terminated 99
Series terminated HSTL bus 155
Series terminated nets 73
Series terminated TL 69
Series terminated 62
Series termination stub 71
Series termination 29
Serpentine tuning/routing 223
Sheet resistance, plane 149
Signal integrity engineering 57
Signal integrity tools 217
Signal loss in traces 190
Signal losses 19
Signal plane fill 167, 171
SIMM 99
Simplified impedance equation 48
Simultaneous switching noise 117, 176
Single ended signaling 112
Single ended 43
Skin effect loss 19, 41
Slew rate 33
Sources 21
Speed of light 33
SPI-4.1 159
SPICE models 217
Spreading resistance 130
SSN 176
SSN 117
SST 99
Stacking stripe 199
Straight wire 223
Stripline transmission line 30
Stripline 44, 83
Stubs 72
Surface microstrip 209
Symmetrical stripline 83
System level checking 218
Tantalum organic capacitor 132
TCE 202
TDR 88
Technology table 195
Teflon 201
TEL 34, 59
Temperature coefficient of exp. 202
Terminator end swapping 72

Terminator noise 191
Terminator stub 70
Test card, capacitor 147
Test point files 226
Tg 201
The impedance equation 80
Thermal offsets 191
Thermal ties 262
Thevenin termination 65
Through hole vias 211
Time and distance 33
Time Domain Reflectometer 88
Timing analysis 186
Timing analysis tools 217
TL 70
Trace DC resistance 191
Transition electrical length 34
Transmission line 43
Transmission lines 21, 25
Trombone tuning/routing 223
TTL engineering 214
Turning via 223
Types of high speed PCBs 18
Typical parallel terminated nets 73
Typical use power 155
Undershoot 51
Unplated holes 262
Unterminated transmission line 52
Vacuum lamination 197
Variable slew rate 33
Vcc bounce 176
Vcc bounce tests 178
Vcc bounce 117
Vcc offsets 188
Velocity of propagation 149
Via types 211
Vias 92
VIH_{MIN} 184
VIL_{MAX} 184
Virtual prototyping 215
Visible vs. Significant 16
VOH_{MAX} 183
VOH_{MIN} 183
VOL_{MAX} 183
VOL_{MIN} 183
Voltage sources 96
Water absorption 205
Why 50 ohms? 86
Wire 223
X7R 132
XAUI 120
X_C 133
X_c 39
X_L 133
X_L 36
X-Y routing 221
Y5V 132
Z axis expansion 203
Z vs. F for 2.5 V supply 166