POWER PLANE THERMAL TIE DESIGN

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The purpose of this applications note is to define what a thermal tie is and how to design it.

DEFINITION: A thermal tie is a connection between a component pin and the power plane in a PCB. Its purpose is to provide a good electrical connection between the pin and the plane while providing a poor thermal connection. Thermal ties are not needed for press fit connectors or surface mount components.

The thermal isolation is required because the component lead must be successfully soldered into the via or plated through hole. If no thermal isolation is provided between the plated through hole and the power plane, heat needed to complete the solder connection will be drawn away from the hole by the plane copper and soldering will not be complete. It is possible to preheat the whole PCB to a temperature that will allow the formation of a good solder connection even without thermal ties. However, if this is done, it will be nearly impossible to unsolder the pin if rework is necessary. The wider each tie is the more thermal loss there will be and the more difficult soldering will be. So, from a solderability point of view, one tie would be best. From a reliability point of view more than one tie would be best. The designer must construct a thermal tie design that makes appropriate, safe compromised between these two objectives.

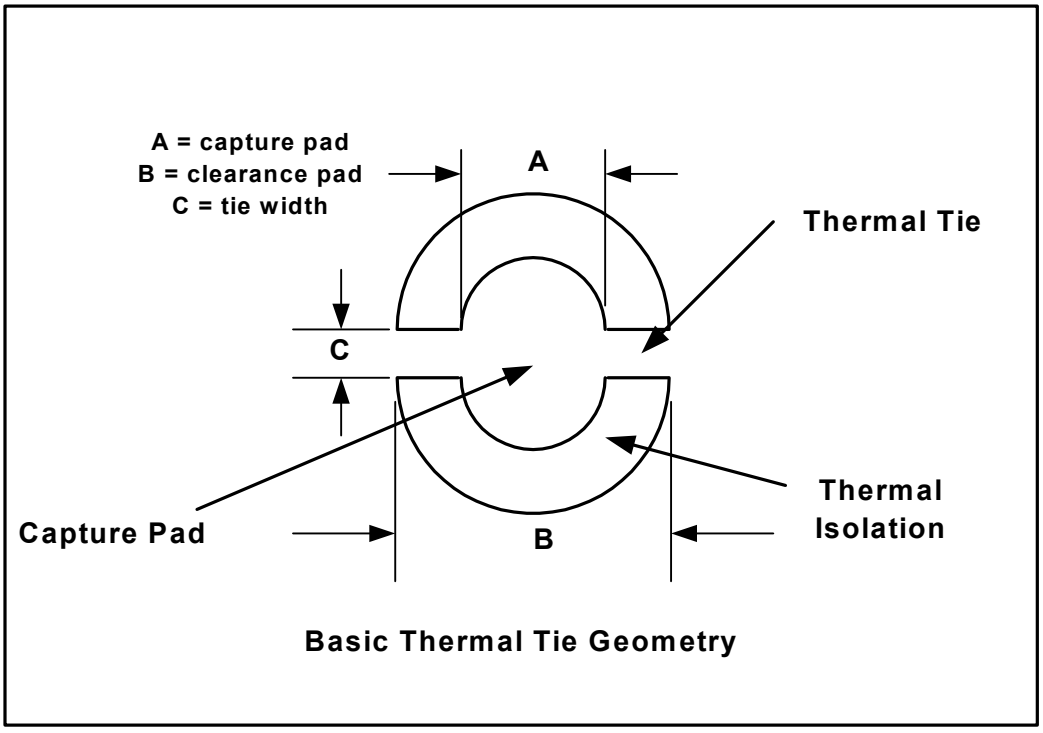

Figure 1, Thermal Tie Geometry

Figure 1 is a common thermal tie design. There exist designs with four ties or spokes. When the reason for the ties or spokes in understood, it will be clear that two ties is enough. **Figure 2** shows the thermal tie structure with the via hole drilled through it. The hole is centered in the pattern as designed.

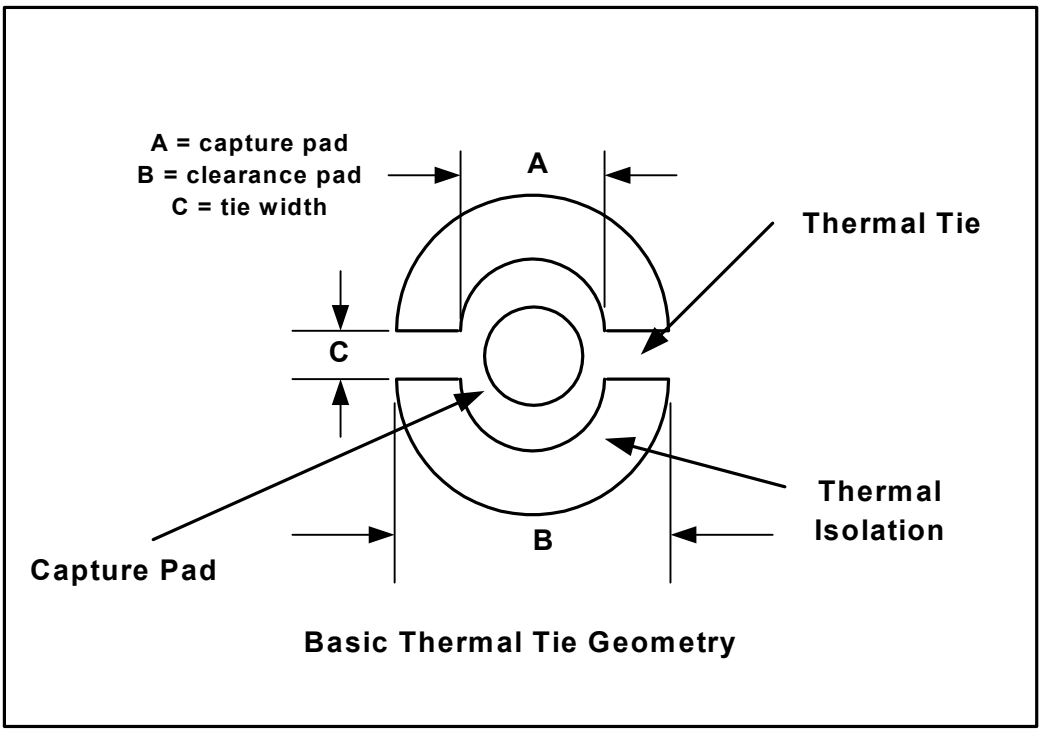

Figure 2, Thermal Tie Structure with via hole drilled into it.

If this condition existed for all holes in a PCB, there would be no need for two ties. Either of the two provides a good electrical connection to the plane. **Figure 3** shows what actually happens in production. Tolerance build up causes some of the holes to be drilled off center. When the hole becomes tangent to the capture pad, the metallic contact between the plated through hole and the tie is only the end on area of the tie. Years of testing have shown that the shock of soldering will break this weak bond and the connection will be intermittent. One solution would be to make the capture pad larger. That works, but the length of the thermal tie is reduced in the process and solderability is compromised. A fix for this might be to increase the size of the clearance pad in the plane. With fine-pitched parts, this is not a choice due to the fact that clearance pads cannot be allowed to overlap on adjacent vias.

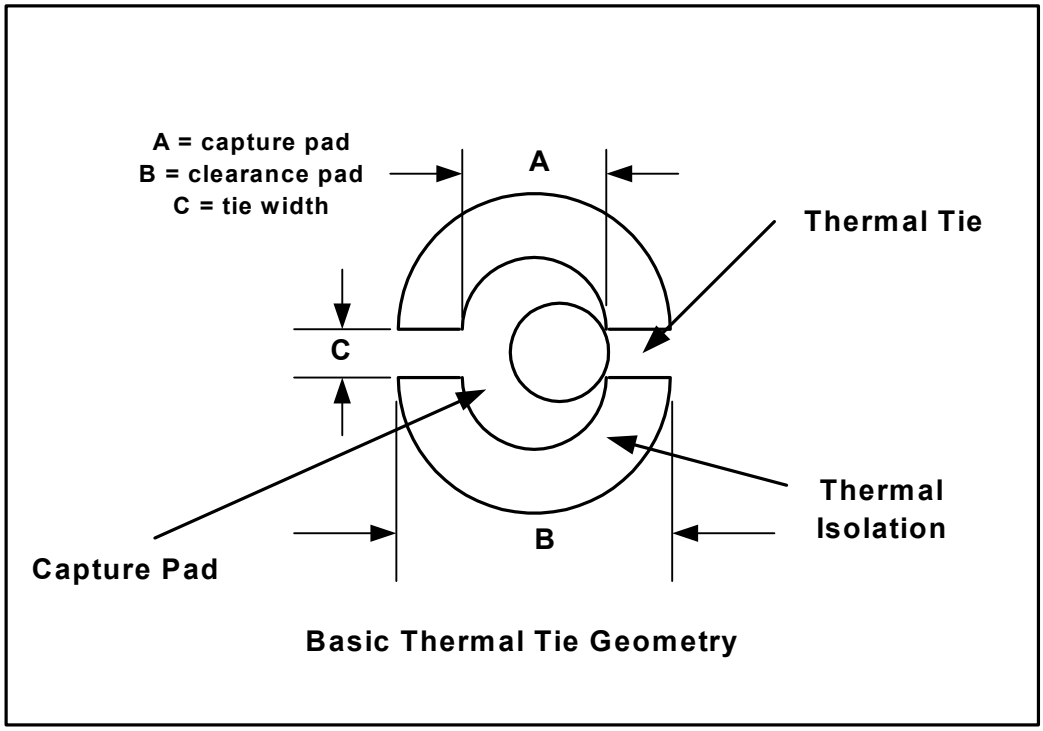

Figure 3, Thermal Tie Structure with hole drilled off center

Adding a second tie insures that there will always be one connection between the plated through hole and the plane that is original foil copper from the plane. Adding more ties, as in the case of the four tie configuration, does not improve reliability, but it does reduce solderability. Therefore, a two tie thermal tie structure is adequate for connecting IC and connector pins to power planes.

Designing a Thermal Tie Structure.

Objectives that must be met when designing a thermal tie structure are:

- Maximize thermal isolation of plated through hole barrel from power plane
- Insure that connection has a low enough DC resistance and AC inductance to satisfy the electrical requirements
- Insure that design is manufacturable and reliable.

The first objective is met by making the tie as long as possible and minimizing its cross section.

The second objective is met by making the tie as short as possible and maximizing its cross section!

The third objective is met by making sure that the thermal isolation ring is large enough to properly etch. $\geq$5 mils.

Where to begin. There are some constraints that can serve as a starting point. First, the diameter of the outer circle, the clearance opening in the plane should be the same diameter as the clearance opening in the plane that was calculated for the hole being drilled. Second, the inner pad or capture pad should be the same size as the capture pad calculated for a signal layer less the annular ring allowance, usually 2 mils per side or four mils.

In almost all cases, the difference in diameter between the two pad sizes noted above will be 10 mils or an isolation width of 5 mils.

All that remains is to select a tie width that satisfies the two conflicting constraints, thermal and electrical. **Chart 1** is a plot of trace resistance vs. trace width and copper thickness. From it we can calculate the resistance of a 5 mil long tie of varying trace width and copper thickness.

Starting with a 5 mil wide trace in 0.5 ounce copper, we can see that this cross section yields about 1.75 ohms per foot or .0002 ohms per mil of length. This would result in a 1 milliohm resistance for a 5 mil long tie, certainly adequate for any power pin of any realistic IC or connector. Therefore, 5 mil wide ties will satisfy the DC electrical requirement. 5 mil wide traces average about 8 nanoheries per inch of length. The 5 mil long tie will be 1/200th of this or .04 nanohenry. This inductance is far below any of the parasitic inductances in the rest of this signal path, so the AC electrical requirement is also met.

The hard question is: does this structure size provide sufficient thermal isolation? Not an easy question to answer. This is best answered by trying to remove a component lead soldered into such a hole. If there are multiple planes connected to the same via, there may be too much thermal leakage.

Drawing from past experience, two thermal ties of the above geometry in 0.5 ounce copper do not represent excessive thermal sinking.

FAQ- Does the orientation of the ties matter? No, so long as the spacing of holes is large enough to guarantee a copper web at least 5 mils wide between adjacent clearance pads.

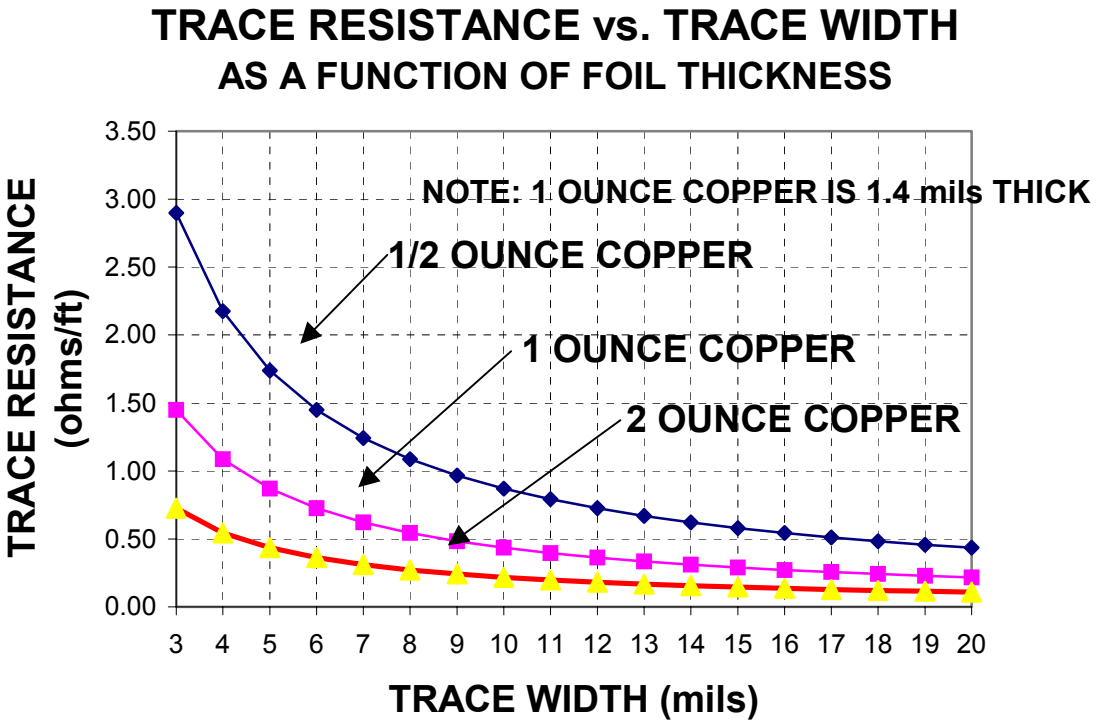

Chart 1, Trace Resistance vs. Trace Width and Copper Thickness.
(1 ounce = 1.4 mils thick)