Article Number	TOPIC	BOOK	TITLE	AUTHOR	PUBLICATION	CC
1	SMT	1	Pick and Place Adds Vision	Ford, Donald	Ckts. Mfg.	Stat
2	CAD	1	Design Service Spotlight on Shared Res.	Editors	PC Design	Stat
3	FAB	1	Design for Fabrication, Panelization	Ross, Roberta	PC Design	Tera
4	FAB	1	Design Rules for Optimized Fabrication	Hunt, Greg	PC Design	Sou
5	FAB	1	Designers Viewpoint, Hole and Pad Size	Jodoin, Claude	PC Design	UTC
6	CAD	1	Naming Conventions for Components	Ritchey, Lee W.	Shared Res.	Sha
7	THERM	1	Cooling High Speed ECL Conventionally	Gupta, Omkarnath	Elect. Prod.	Fair
8	DES	1	Standard Shared Res. Fine Line Multilayer Package	Ritchey, Lee W.	Shared Res.	Sha
9	DES	1	The Impact of VLSI on PCB Design	Ritchey, Lee W.	VLSI Systems	Sha
10	DES	1	Multilayer Test Coupon Specification	Ritchey, Lee W.	Shared Res.	Sha
11	CAD	1	A Comparison of PCB Routing Methods	Ritchey, Lee W.	PC Design	Sha
12	FAB	1	Implementing ECOs on Multilayer PCBs	McCarthy, Kevin	PC FAB	NEA
13	PKG	1	VLSI Packages: PGAs or Chip Carriers	Balde, John W.	Circuits Mfg.	IEE
14	CAD	1	Real World Constraints on PCB CAD Performance	Keeler, Robert	EP&P	Stat
15	DES	1	Procedure for Creating Netlists from Schematics	Ritchey, Lee W.	Shared Res.	Sha
16	CAD	1	Speedy Gridless Router Designs Denser PCBs	McCloud, Jonah	Electronics	Stat
17	CAD	1	Routing Your Way Through PCB Design Tools	Milne, Bob	Elect. Design	Stat
18	CAD	1	Valid Logic to SR Interface/conversions	Wong, Robert	Shared Res.	Sha
19	CAD	1	Crystal PCB Design System Data Sheet	Ritchey, Lee W.	Shared Res.	Sha
20	DES	1	Impact of New Design Tools on PCB Design & Matls.	Messner, George M	PC Design	PCk
21	CAD	1	A Specialized Router for High Density PCBs	Ho, etal	PC Design	Scic
22	IMP	1	Controlled Impedance. What is it? Who needs it?	Ritchey, Lee W.	Nepcon 1988	Sha
23	XMIS	1	Technology Management and ECL Rules	Ritchey, Lee W.	Shared Res.	Sha
24	PKG	1	Packaging High Speed Circuits	Messner, George M	Ckts Mfg.	PCk
25	XMIS	1	Spice Model & CKT Eff. for High Speed Design	Smith, Mango, etal	IPC Tech Rvw	Ray
26	FAB	1	Electrical and Mechanical Constraints for Low End PCBs	Arthur, David J.	IPC Tech Rvw	Roc
27	XMIS	1	Reflection & Crosstalk in Logic Circuits	DeFalco, John A.	IEEE Spectrum	Hor
28	XMIS	1	Designing Transmission Lines in Multilayer PCBs	Springfield, William I	Electronics	IBM
29	XMIS	1	Microstrip Plus Equations Add up to Fast Design	Schwarzmann, Alfre	Electronics	RCA
30	XMIS	1	Getting a Handle on Impedance, Xtalk, TD, Ringing	Wexler, Al	PC Design	Qua
31	XMIS	1	High Frequency ECL Design	Winchester, Elizabe	PC Design	Tele

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32	XMIS	1	Stubs Affect PCB Performance	Malack, etal	EP&P	IBM
33	FAB	1	Understanding the Manufacturing Process	Sanscrainte, Ren	PC Design	Dav
34	FAB	1	Paint it All Black (copper treatment)	Johnson, Daniel G.	Ckts Mfg.	Shi
35	CAD	1	The State of Drill Tapes	Ritchey, Lee W.	PC Fab	Sha
36	FAB	1	How Tolerable are PCB Tolerances?	Doyle, etal	Ckts Mfg.	CD(
37	FAB	1	Small Hole Drilling, Fine Points Make a Difference	Tuck, John	Ckts Mfg.	Stat
38	DES	1	Fabrication Driven Design, Part 1	Falque, Terry etal	PC Design	ASI
39	DES	1	Fabrication Driven Design, Part 2	Falque, Terry etal	PC Design	ASI
40	DES	1	Fabrication Driven Design, Part 3	Falque, Terry etal	PC Design	ASI
41	FAB	1	Film Dimensional Changes	Irving, Shannon	IPC Tech Revw	HP
42	FAB	1	Vapor Phase Curing of Dolder Masks	WHM		
43	RES	1	Planar Resistor Technology for High Speed PCBs	Mahler, Bruce	EP&P	Ohr
44	RES	1	Thin Film Resistor Technology	Mahler, Bruce	PC Design	Ohr
45	ASSY	1	A Design Guide to Soldering, Part 1	Woodgate, Ralph	PC Design	Wo(
46	FAB	1	The Spread of Liquid Soldermasks	Denkler, John D.	Ckts Mfg.	M&T
47	SMT	1	Design Considerations for SMT Assemblies	Marcoux, Phil P.	PC Design	PPM
48	SMT	1	Surface Mount Design	Blankenhorn, James	PC Design	SM
49	SMT	1	Does Surface Mount Make Sense for VLSI Designs?	Ritchey, Lee W.	VLSI Systems	Sha
50	SMT	1	SMT Autorouting for High Density Applications	Rygiol, Jim	PC Design	PCI
51	SMT	1	Surface Mount CAD Design	Skomp, Greg	PC Design	Cac
52	SMT	1	Selecting a Product for Using SMT Technolgoy	Blankenhorn, James	PC Design	SM
53	SMT	1	The Impact of SMT on CAD	Rygiol, Jim	PC Design	Cac
54	SMT	1	Design Guidelines for SMT	Solberg, Vern	PC Design	NuC
55	CAD	1	Survey of PCB CAD Systems	Editors	VLSI Systems	Stat
56	DES	1	Supercomputers, the Proliferation Begins	Editors	Electronics	Stat
57	FAB	1	1988 PCB Pricing Guide	Esposito, Donna	PC Fab	PC
58	CAD	1	Designers Guide to PCB CAD Systems	Editors	Comp. Design	Stat
59	CAD	1	Designers Guide to Simulators	Editors	Comp. Design	Stat
60	CAD	2	Designers Guide to Schematic Capture	Editors	Comp. Design	Stat
61	TAB	2	TAB Tames High Density Chip I/Os	Markstein, Howard	EP&P	Stat
62	FAB	2	Tricks to Manufacturing Metal Core PCBs	Smith-Vargo, Linda	EP&P	Stat
63	MCM	2	Chip on Board Technology	Neilsen, Arne	PC Fab	Valt

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64	MATL	2	Specialty Laminates Fill Special Needs	Spitz, Leonard	EP&P	
65	FAB	2	Technical Cost Modeling	Ng, Lee etal	PC Fab	MIT
66	SMT	2	SMT Cures PCB Problems	Ritchey, Lee W.	High Perf Sys	Sha
67	SMT	2	Stretching the Limits of SMT Placement	Mullen, Don etal	EP&P	Eva
68	SMT	2	Same article as 66			
69	XMIS	2	Technology Table Explain w/Seq. Definitions	Ritchey, Lee W.	Shared Res.	Sha
70	SMT	2	SMT Demands on PCB Substrates	Ibrahim, Muhammad	PC Fab	Mar
71	SMT	2	Substrate Selection for SMT Compatibility	Huschka, Manfred	PC Fab	Nor
72	FAB	2	The Impact of Metal Core Boards	Wilson, Geoffrey	PC Fab	Fer
73	FAB	2	Multilayer PCB Manufacturing	Douglas, Richard R.	PC Fab	Cor
74	XMIS	2	Model Timing Eases Design of High Speed PCBs	Meyer, Ernest	Comp Design	Stat
75	CAD	2	PCB CAD Libraries Struggle to Support Design	Meyer, Ernest	Comp Design	Stat
76	CAD	2	High End Tools for PCB Design Evolve	Gabay, John	EE Times	Stat
77	IMP	2	Who is Responsible for Controlled Impedance?	Ritchey, Lee W.	PC Fab	Sha
78	DES	2	Circuit Designer's Focus Group Meeting, w/Lee Ritchey	Knack, Kella	Circuit Design	Stat
79	DES	2	Maintaining Balance in Complex PCB Design	Murphy, Daniel W.	High Perf Sys	Sha
80	XMIS	2	Fast Bus Interface Chips Tackle Tough System Design	Bursky, Dave	Elect. Design	Stat
81	MCM	2	Bare Chip Packaging	Busby, Mike	High Perf Sys	Uni
82	MATL	2	A New Low Dielectric Material for PCBs (PTFE & resin)	Snyder, William W.	PC Fab	Gor
83	DES	2	Characteristics of Four Large Multilayer PCBs	Murphy, Daniel W. e	Circuit Design	Sha
84	CAD	2	What Do Your Design Tools Really Cost?	Arnold, Bill	ASIC Tech & N	Stat
85	CAD	2	PCB Placement Tool Offers Net Sequencing (Mentor)	Editor	High Perf Sys	Stat
86	CAD	2	Analysis Tool Hits Market, Crystal	Wirbel, Loring	EE Times	Stat
87	CAD	2	PCB Software Has Expanded Capabilities (Crystal)	Editor	Elect Prod	Stat
88	DES	2	Complex PCB Design Methodology, Part 1	Ritchey, Lee W.	PC Design	Sha
89	DES	2	Complex PCB Design Methodology, Part 2	Ritchey, Lee W.	PC Design	Sha
90	XMIS	2	CAE Tools Help Cure Xmission Line Woes	Quinell, Richard A.	EDN	Stat
91	CAD	2	Designers Discover Tools for PCB Layout Hazards	Donlin, Mike	Comp Design	Stat
92	SMT	2	Designing SMT PCBs for Testability	Ritchey, Lee W.	PC Design	Sha
93	MCM	3	Chip on Board Packaging	Ritchey, Lee W.	PC Design	Sha
94	XMIS	3	A Test PCB to Evaluate Vias, Bends, est.	Ritchey, Lee W. etal	IPC Proceding	Sha
95	IMP	3	Controlled Impedance in PCB Design & Fab.	Ritchey, Lee W.	PCB Expo 89	Sha

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96	IMP	3	Controlled Impedance Design	Ritchey, Lee W.	PC Design	Sha
97	XMIS	3	Transmission Line Sequencing in High Speed Design	Ritchey, Lee W.	High Perf Sys	Sha
98	CAD	3	The Role of Crystal Placement in PCB Design	Ritchey, Lee W.	Shared Res	Sha
99	DES	3	PCB Design, in house or out?	Ritchey, Lee W.	Comp Design Nv	Sha
100	XMIS	3	High Speed PCB Design	Ritchey, Lee W.	SmI Procedings	Sha
101	XMIS	3	High Speed Design Paper	Ritchey, Lee W.	IDEA 91	Sha
102	MCM	3	Multichip Module Design & Test	Ritchey, Lee W.	Shared Res.	Sha
103	SMT	3	SMT Component Library Design	Ritchey, Lee W.	Shared Res.	Sha
104	IMP	3	Creating Zo test Lines in PCBs	Ritchey, Lee W.	Shared Res.	Sha
105	TEST	3	Testing Loaded Double Sided PCBs	Ritchey, Lee W.	Shared Res.	Sha
106	CAD	3	Standard Shared Resources Data Formats	Ritchey, Lee W.	Shared Res.	Sha
107	COUP	3	Trace to Trace Coupling	Ritchey, Lee W.	Shared Res.	Sha
108	DES	3	First, Do No Harm Guest Editorial	Ritchey, Lee W.	PC Design	Sha
109	XMIS	3	Layout, Coupling and Impedance Rules for PCB Design	Ritchey, Lee W.	PCB Design Cor	Sha
110	DES	3	Lazy Man's Guide to SMT PCB Design	Ritchey, Lee W.	High Perf Sys	Sha
111	CAPS	4	Eliminating Capacitors from Multilayer PCBs	Sisler, Joh	PC Design	Uns
112	CAD	4	Optimizing Autorouting Boosts PCB Manufacturability	Mantay, L.A. etal	EP&P	AT&
113	MCM	4	MCMs, many Options, Many Questions	Costlow, Terry	EE Times	Stat
114	MCM	4	Design Tools Cope With MCM Challenges	Isaac, John	EE Times	Stat
115	IMP	4	Fabricated PCB Charateristics & Zo Tests	Parkinson, Harry E.	Digital	DEC
116	DES	4	Designers Rountable, Lee Ritchey	Waddell, Pete	PC Design	Stat
117	XMIS	4	Packaging for High Speed	Markstein, Howard	EP&P	Stat
118	XMIS	4	Matched Impedance Transmission Line Options	Rosen, Richard P.	EP&P	MM
119	XMIS	4	A High Speed Approach to Controlled Zo Packaging	Kozuch, John J.	Multiwire	Mul
120	MATL	4	A New Low Dielectric Material for PCBs	Snyder, William W.	PC Fab	Gor
121	BUS	4	Fast Bus Interface ICs Tackle Tough System Design	Bursky, Dave	Elect Design	Stat
122	FAB	4	The Case for Tented Vias	Maki, Jon R.	PC Fab	Har
123	FAB	4	PCB Layer Counts Not Always Key Cost	Mayer, John	Comp Design	Stat
124	RES	4	Planar Resistor Technology for High Speed PCBs	Mahler, Bruce		Ohr
125	RES	4	Resistor Packaging Options: To Bury or Not	Snyder, Kenneth C.	PC Design	Plar
126	XMIS	4	High Speed Interconnect Design Methodology	Cutler & Snyder	Circuit Design	C&C
127	FAB	4	Multiwire Today	Kunkle, Robert E.	PC Fab	I-Cc

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128	CAD	4	CAE Vendors Strive to Improve Link, Design to Layout	Donlin, Mike	Comp Design	Stat
129	DES	4	Playing by the Rules	Ritchey, Lee W.	Comp Design	Sha
130	MCM	4	Intel Rolls Dice for MCM Makers	Costlow, Terry	EE Times	Stat
131	IMP	4	Controlled Impedance - The Design Problem & Tool	Ritchey, Lee W.	Seminar?	
132	FAB	4	PCB Vendor Survey Procedure	Ritchey, Lee W.	Shared Res.	Sha
133	MATL	5	Measuring Relative Dielectric Constant of PCB Lams	Ritchey, Lee W.	Circuitree	Sha
134	FAB	5	No Paper			
135	MATL	5	Hercules Polyclad "Sycar" FR-511 Resin Sys	Ritchey, Lee W.	Shared Res.	Sha
136	MATL	5	Polyclad Introduces PCL-511 Laminate	Whitehouse, Roger	Circuitree	Stat
137	MCM	5	Bare Chip Packaging	Busby, Mike	High Perf Sys	Unis
138	IMP	5	Magnuson PCB Impedance Report	Ritchey, Lee W.	Magnuson	Mag
139	FAB	5	Hitachi Multiwire Process Chart & Brochure		Hitachi	Hita
140	XMIS	5	High Frequency Crosstalk & Impedance in PCBs	Delabre, W. etal	IPC	U of
141	DES	5	Adapt Your Engineering Process, Guest Editorial	Ritchey, Lee W.	Comp Design	Sha
142	COUP	5	Coupling Analysis Sketch for ELXSI	Ritchey, Lee W.	Shared Res.	Sha
143	IMP	5	Controlled Impedance Spec for PCBs, From DEC		DEC	DEC
144	IMP	5	Controlled Impedance Test Spec from DEC		DEC	DEC
145	FAB	5	PCB Stackup from 4 to 16 Layers	Ritchey, Lee W.	Shared Res.	Sha
146	FAB	5	Fine Line Etching	Letize, Ray	PC FAB	Mac
147	CONN	5	Are Screw Machine Sockets Necessary. Rel. Study	Tecsy, Miklos	Magnuson	Mag
148	FAB	5	Plating Small Holes, Good Hole Cross Section	Hastie, William M.	Circuits Mfg.	Stat
149	FAB	5	PCB Fabrication Spec.	Ritchey & Young	Magnuson	Mag
150	DES	5	Control the PCB Thru the Design, Fab & Mfg. Good PIX	Holcomb, William P.	PC Fab	Sing
151	FAB	5	A Multilayer Primer, Fab Process, Laminates	McGowan, Davide R	PC Fab	Poly
152	FAB	5	A Good Color Shot of a Plated Through Hole			
153	MCM	5	Interconnecting Chip Carriers: A Review	Dance, Frances J.	Ckts Mfg.	TI
154	DES	5	The Language of Printed Circuits, a Glossary	Staff	PC Fab	Nat
155	MCM	5	MCMs Hit the Road, A Special Report	Derman, Glenda	EE Times	Stat
156	MATL	5	A New Low Er Material, Herc/Sycar/Poly-FR-511		Hercules	Stat
157	MATL	5	Controlled Impedance Materials, Great Materials Charts	Lewis, Ed	SMI 1991	ADI
158	IMP	5	Computer Testing for Zo	Currier, Dal	SMT 1991	Aml
159	FAB	5	Software Based PCB Cost Model	Donneley, Ed	SMI 1991	BPA

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160	MCM	5	Design for Manufacturability of MCMs	Ives, Debora	IPC Tech Revw	Cac
161	FAB	5	Solder Masks	Ritchey, Lee W.	Share dRes.	Sha
162	IMP	5	Differential TDR Testing Techniques	Theorin, etal	Connector Tech	Gor
163	IMP	5	Controlled Impedance in PCBs, a Good Study of Equat.	Lerch, Carolyn	PC Fab	Psi
164	IMP	5	Practical Design for Controlled Zo, a Good Primer	Canright, Robert	IEE, ECTC	Mar
165	IMP	5	Advanced Interconnect for High Speed, Good Diagrams	Mango, Ricci, etal	GOMAC	Ray
166	IMP	5	Comments on Analytical Alg, for Unbalanced Stripline	Canright, Robert		Mar
167	IMP	5	An Analog Algorithm for Unbalanced Stripline	Robrish, Peter	IEEE Trans	HP
168	IMP	5	A Formula for Dual Stripline	Canright, Robert	IEEE Proc	Mar
169	IMP	5	Impact of High Speed Circuits on PCBs	Canright, Robert	IPC TMRC	Mar
170	MATL	5	POLYHIC Behavior at High Frequencies, a material	Bradner etal	IEEE/ECC	AT&
171	IMP	5	Maximizing Tolerances for PCB Characteristic Imped.	Canright, Robert	IEEE/CHMT	Mar
172	IMP	5	Packaging High Speed Dig, Sys, on Mantech Equation	Canright, Robert	Martin Mariet	Mar
173	IMP	5	Equations for Crosstalk and Impedance	Canright, Robert	IEPS	Mar
174	FAB	5	A Note on All Pads Outer Layers	Ritchey, Lee W.	Shared Res.	Sha
175	FAB	5	Quickturn backplane Hole Fractures, shows HASL			
176	FAB	5	Surface Mount Tackles Fine Pitches, Good Photos	Maliniak, David	Elec Design	Stat
177	SMT	5	Fabrication Tolerances from Aeroscientific		Aero	
178	XMIS	5	Transmission Line Simulation Needs Refining	Ritchey, Lee W.	Shared Res.	Sha
179	XMIS	5	New Termination Approach, Diodes on SCSI	Costlow, Terry	EE Times	Stat
180	CONN	6	Optimizing SI in HIgh Speed Connectors	Zanells, Fab etal	EP&P	Ter
181	DES	6	System Timing Bar Chart 33 MHz/66 MHz	EE Times		
182	DES	6	Rajan's SPQL Equations	Varadarajan, R		
183	EMI	6	EMI Suppression Techniques for PCBs	Montrose, M	Montrose	Mor
184	DES	6	Disc Drive Block Diagram	Maxtor	Maxtor	Max
185	DES	6	Tackling High Speed Designs	Ritchey, Lee W.	EE Times	Sha
186	ASSY	6	COB Encapsulants	Swanson, Dale	Adv. Pkg	Abe
187	MVIA	6	Maximizing PCB Real Estate with Blind Vias	Luciano, Dante	SMT	Hac
188	DES	6	BICMOS Buys Back 3V Performance	Morris, Bernie	ASIC & EDA	ATT
189	DES	6	Steam Engine Whistle Design	Mims, Forrest	POP ELECT	
190	MFG	6	Tips to Cost Effective Flexible Manufacturing	Staff	ELEC BUS	Stat
191	CONN	6	Fretting Corrosion in Electrical Contacts	Whitley, James	AMP	AMI

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192	MFG	6	Can Burn in Cause Problems?	?	EVAL ENG	?
193	DES	6	Using Your Oscilloscope Probe	Tektronix	TEK	?
194	MFG	6	Microcircuit Reliabiliy Assessment thru Accel	Lehtonen, David	Motorola	Mot
195	ESD	6	Control of ESD Damage to Semiconductors	Freeman etal	IEEE REL	Mar
196	XMIS	6	Transmission Line Effects in PCB Applications	Staff	Motorola	Mot
197	TEST	6	Why is Testability Important?	Wyatt, Mike	Maxtor	Max
198	TEST	6	Follow These Guidelins to Design Testable ***	Venkat, Kumar	EDN	Sil.
199	SI	6	Signal Analysis: A Must for PCB Design Success, SI Tools	Maliniak, Lisa	ELEC DES	Stat
200	DES	6	What is an Engineering Drawing?	Ritchey, Lee W.	Shared Res.	Sha
201	DES	6	Thermal Tie Resistance Analysis	Ritchey, Lee W.	Shared Res.	Sha
202	DES	6	Automation Drives PCB Success, Design Process Story	Lombard, Tim	PC Design	CIS
203	MFG	6	How Much Fault Coverage is Enough?	??	EDN	??
204	TEST	6	Analysis of Test Cost vs. Test Coverage	??	??	??
205	DES	6	Table of Metric vs. English Dimensions	Ritchey, Lee W.	??	??
206	CAPS	6	Power Bus Decoupling on Multilayer PCB, great article	Hubing, etal	IEEE	UMI
207	XMIS	6	Effects of Vias on PCB Traces, good study	Brooks, Doug	Ultracad	Ultr
208	FAB	6	Table of PCB Tolerances, good table	Multek	Multek	Mul
209	DES	6	Strategies for High Speed Circuit Design	Meyer,Ernest	ASIC & EDA	Stat
210	DES	6	Debunking High Speed PCB Design Myths	Knack, Kella	ASIC & EDA	Stat
211	DES	6	What's Good Enough? High Speed Design Rules	Ritchey, Lee W.	ASIC & EDA	3CC
212	XMIS	6	Interconnect Utility Disc Data Sheet	Cutler, Robert	Cutler	Cutl
213	FAB	6	Leaving It Up to the FAB Shop and Other Dangerous Behav.	Ritchey, Lee W.	Circuitree	3CC
214	IMP	6	Why do we have so Much Trouble Getting the Impedance?	Ritchey, Lee W.	Circuitree	3CC
215	EMI	6	Use Simulation to Spot and Fix EMI Problems	Lam & Powell	Elec Desgn	Qua
216	EMUL	6	Pentium Design Using Quickturn Emulation	Wilson, Ron	EE Times	Stat
217	DES	6	Designers Consider Test Economics for ASICS	Runyon, Stann	EE Times	Stat
218	DES	6	What Do Your Design Tools Really Cost?	Arnold	Bill	Stat
219	SI	6	Analysis Tools Target Early Stages of PCB Design	Donlin, Mike	Comp Desgn	Stat
220	DES	6	High Speed- Mainstream Design Technology, Lee R. parts	Blanchard, Dave	PC Design	Stat
221	CONN	6	PC Card Connector Suppliers		Elec Desgn	Stat
222	CONN	6	SCSI Connectors Close the EMI/RFI Gap	Thornton, Bob	Elec Desgn	Fuji
223	DES	6	Job Process Check List	Shared	Shared	Sha
224	XMIS	6	SMT+ Controlled Impedance Analyser Data Sheet	Blankenhorn, Jim	SMT+	SM
225	EMI	6	Remove Mistique of EMI Suppression in Wireless Application	Kakad etal	Wireless Sys	Gor

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226	DES	6	Tools and Teamwork are key to Successful PCB Design	Staff	Comp Desgn	Stat
227	DES	6	List of Reference Materials for PCB Design	Ritchey, Lee W.		3CC
228	DES	6	Current Carrying Capacity of Copper Conductors	Grundy, Felton	3COM	3CC
229	BUS	6	History/Commercial Usage of GTL	Staff	TI	TI
230	MFG	6	Universal Disc Drive Tester Specification	Staff	Maxtor	Max
231	CONN	7	High Performance Connectors- Gnr to signal patterns	Modinger etal	Elect Desgn	ERN
232	PWRS	7	Advanced Micros Demand High Current at < 2V	Goodenough, F	Elect Desgn	?
233	PWRS	7	Designing Power Systems Around Processor Applications	Goodfellow etal	ELect Desgn	Inte
234	MATL	7	Breakthrough Improvements in Dim. Perf. of Thin Laminates	Feeney, James	Circuitree	Mas
235	EMI	7	Keep Those Switchers Quiet, EMI Suppression	Leman, Brooks	Port Desgn	Pow
236	MATL	7	Permittivity/Dielectric Constant:Do the Math	Neves, Bob	Circuitree	Mic
237	XMIS	7	Controlled Impedance and the TDR	Neves, Bob	Circuitree	Mic
238	FAB	7	Selecting the Appropriate Test Pattern for Fab Defect	Rhodes, Ron	Circuitree	CAT
239	CAP	7	Distributed Capacitance Technology, Good Z vs F curves	Howard, James	Zycon	Zyc
240	RES	7	Characterization of Integrated Resistors for PCBs	Peeters etal	Zycon	Zyc
241	FAB	7	Flexible Circuits, Design for the Application	Hitchcock, etal	Merix	Mer
242	BGA	7	A Practical Guide to BGA Assembly	Solberg, Vern	Tessera	Tes
243	FAB	7	A Primer on Drill Bits	Staff	EP&P	Stat
244	FAB	7	A Collection of Drilled Hole Cross Sections, GOOD	Staff	Circuitree	Stat
245	MATL	7	RO4000 Performance Specifications	Rogers	Circuitree	Rog
246	DES	7	High Fashion is High Tech	Costello, Joe	Elect Bus	Cac
247	MVIA	7	Laser Ablated Blind Via Design Guide	Hu, Mason	Zycon	Zyc
248	DES	7	Ground Bounce Tests Good Scope Tracings	Shear, David	EDN	Stat
249	MVIA	7	Substrate Technology Reduces BGA Cost, Microvias	Wu, Paul	EP&P	Pro
250	CONN	7	High Performance Connectors- The Weak Link	Modinger, etal	Elect Desgn	ERN
251	CONN	7	Manufacturers of Board Level Connectors	Staff	Elect Desgn	Stat
252	SI	7	EDA Tools, a List of Layout, SI, etc. Tools	Goering, Richard	EE Times	EE
253	DES	7	Pushing the Ethernet Envelope, Gigabit ENET Paper	Johnson, Howard	PC Design	Sig
254	TEST	7	Production Test System Enhancements Reduce ATE Costs	Staff	Elect Prod	Stat
255	PWRS	7	Design Power Systems Around Processor Specifications	Goodfellow, etal	Elect Desgn	Inte
256	MCM	7	Low Cost Organic Packaging for High Performance MCMs	Dudeck, Gary	EP&P	Mic
257	CAPS	7	OperatingAbove Resonance, a Bypass Capacitor Paper	Johnson, Howard	Elect Desgn	Sig
258	DES	7	PCB and IC Design Software, Layout Tools List	Clarkson, Mark	Desktop Eng	Stat
259	MATL	7	Primer on HighPerformance Laminates with Cost & Property	Neusch, Martin	EP&P	Poly
260	EMI	7	Proper Shielding reduces EMI, Lists shielding Materials	Markstein, Howard	EP&P	Stat
261	DES	7	Probing High Speed Designs, Good on Scope Probes	Johnson, Howard	Elect Desgn	Sig
262	DES	7	A Novel Right Angle LED	Kornoski etal	SMT	Mot

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263	TEST	7	Test Your Spread Spectrum Products	Schwarts, Richard	Test & Meas	Sigt
264	EMI	7	Learn to Live with the European Directive	Strassberg, Dan	EDN	Stat
265	BGA	7	Self Centering of BGAs and Solder Interconnects	Greathouse, Steve	EP&P	Inte
266	DES	7	Wireless System Design- New Hope for the RF Challenged	Goldberg, Lee	Elect Desgn	Stat
267	EMI	7	The CE Marking: Separating Fact from Fiction	Lohbeck, David	EDN	TU\
268	BGA	7	Build up Laminates Used in High Density Applications BGAs	Chillara etal	EP&P	Fuji
269	SI	7	Planning for Signal Integrity, SI Modelling	Johnson, Howard	Elect Desgn	Sig
270	SI	7	The I/O Buffer Information Specification IBIS	Johnson, Howard	PC Design	Sig
271	BGA	7	Incorporating BGAs into High Volume Operations, GOOD	Partridge, Julian	EP&P	XeT
272	FAB	7	Documenting a PCB Design to Get it Built Right & Verifiable	Ritchey, Lee W.	Circuitree	3C
273	XMIS	7	2D Field Solvers and Predicting Impedance	Ritchey, Lee W.	Circuitree	3C
274	FAB	7	Oh, Lord, We Forgot Our Map andWe're Stuck in Lodi Stack	Ritchey, Lee W.	Circuitree	3C
275	SI	7	Proven Methods Assure Signal Integrity	Ritchey, Lee W.	EE Times	3C
276	EMI	8	Computer Simulation avoids EMI/EMC Problems in IC Pkgs	Zoltan, etal	EDN	Ans
277	XMIS	8	Take The Mystery Out of AC Termination	Nemec, John	ELEC DES	Cal
278	XMIS	8	Slot Antennas from Fields & Waves	Holt	Wiley	
279	BGA	8	Ball Grid Array Socket and Probing System		Emul Tech	
280	MVIA	8	Laser MicroVia Drilling in Circuit Boards	Cable, Alan	Circuitree	ESI
281	BGA	8	BGA, MicroBGA, Chip Scale Packaging at USR	Evans, etal		USI
282	MVIA	8	Laser Ablade Blind Via Design Guideline	Hu, Mason	Zycon	Zyc
283	XMIS	8	Stripline Filter Design from Microwave Eng Handbook			
284	FAB	8	Diagrams of Etching Undercut on Outer Layers	Unk	Unk	Unk
285	DES	8	Fairchild Logic Selection Guide with IC Properties	Unk	Fairchild	Fair
286	MVIA	8	Lumonics Laser Drill Data Sheet	Unk	Lumonics	Lum
287	DES	8	Connectix Design Data Entry Sheets	Unk	Mentor	
288	BUS	8	PCI Bus Design Specification	Unk		
289	BUS	8	LVDS Rreports for Bus Duty (National ICs)	Child, Jeff	Elect Design	Ele
290	FAB	8	Fine Lines in Sequential Build Up of PCBs	Dietz, Karl H.	Circuitree	Dup
291	BUS	8	Optimizing PCI Throughout	Staff	EDN	EDI
292	MVIA	8	The Ultimate Board, a Study of Laser Vias vs. Build Up	Smedley, Rick etal	IPC	Circ
293	MVIA	8	HDIS Using Laser Ablated Vias	Hu, Mason	Hadco	Circ
294	MVIA	8	The Practical Application of Microvia Technology	McDermott, Brian	MicroVia Inc.	Circ
295	SI	8	Simulation and Analysis Tools	Ritchey, Lee W.	3COM	PCI
296	DES	8	Timing Your PCB Design	Messina, Bruno A.	Cadence	PCI
297	SI	8	IBIS Model Accuracy	Edlund, Greg	Cray/SGI	PCI
298	SI	8	Signal Integrity, Why You Should Care About It	Doyle, Greg etal	Interconnectix	PCI
299	DES	8	Bypass Capacitors, A Conversation with Todd Hubing	Brooks, Doug	Ultracad	PCI

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300	XMIS	8	Terminating traces on High Speed PCBs	Kaufer, Steve, etal	HyperLynx	PCI
301	IMP	8	PCB Impedance Control	Brooks, Doug	Ultracad	PCI
302	XMIS	8	Crosstalk and Coupling , a Silent Problem	Ritchey, Lee W.	3COM	PCI
303	FAB	8	Understanding Surface Finishes	Prasad, Ray P.	Ray Prasad	SM
304	DES	8	Trace Currents and Temperatures	Brooks, Doug	Ultracad	PCI
305	BUS	8	SSTL Bus Standard EIA/JEDEC EIA/JESD8-8	Staff	EIA/JEDEC	EIA
306	MATL	8	Electrical Characteristics of HS TLs w/Various Diel, good	Montgomery, Eric	Litton	IPC
307	DES	8	Low Skew Clock Driver Data Sheet	Staff	Qual Semi	
308	DES	8	RF/Microwave BreadboardingTechniques	Burns, Lawrence M	3COM	3CC
309	XMIS	8	Mutual Understanding, Connector Cross talk	Johnson, Howard	Sigcon	EDI
310	XMIS	8	Analysis of Image Planes in PCBs (Bad stuff)	Montrose, Mark	MCS	IEE
311	MATL	8	Copper Clad Laminates and Consumer Electronic Trends	Aoki, Masamitsu		Circ
312	MCM	8	New Build-Up PWB for Flip Chip Attach, Thermosetting	Iketani, etal		Circ
313	CAPS	8	Modelling Power Bus Decouplining in Multilayer PCBs	Drewniak etal	UMR	
314	BUS	8	CAD Files for Fab and Assy, 3COM List	Gordon, Mike	3COM	3CC
315	DES	9	Collective Design Advances IC Packaging	Bergman, Dieter	IPC	Elec
316	PKG	9	IC Demands Force Concurrent Engineering	Mannion, Patrick	Elect Design	Elec
317	DES	9	Feeding the Terabit Monster: Gigabit Networking and Beyo	Goldberg, Lee	Elect Design	Elec
318	PKG	9	Packaging Takes Center Stage in IC Design	Lamson, Michael	TI	Elec
319	BUS	9	The Death of PCI	Alderman, Ray	VITA	Elec
320	BUS	9	A Choice for Future Mainstream Memory is Clear RamBus	Gilligham, Peter	MOSAID	Con
321	SI	9	Building a Signal Integrity Department	Johnson, Howard	Sigcon	EDI
322	SI	9	Simulation & Analysis Tools Roundup	Blanchard, Dave	PC Design	PC
323	DES	9	Microwave Structures on PCBs	Burns, Lawrence M	3Com	PC
324	DES	9	Designer's Roundtable, Interview with Lee Ritchey	Lester, Nick	PC Design	PC
325	TEST	9	Electrical Test of HDI PCBs	Vaucher, Christofe	Circuitree	Circ
326	IMP	9	Balancing the Density Equation, PCB trace and spaces	Holden, Happy	Merix	Circ
327	FAB	9	Fine Lines in High Yield PCBs	Dietz, Karl H.	Dupont	Circ
328	XMIS	9	Differential Impedance	Brooks, Doug	Ultracad	PC
329	MVIA	9	Integrating Hi Density Microvia Technology into MLB Fab	Paulus, et al	U of Wisc	Circ
330	DES	9	Getting High Speed PCBs to Market on Time, SI tools	Doyle, Greg etal	Mentor	PC
331	PKG	9	IC Packaging Outlook, Consumption by Type and Year	Berry, Steve	Elect Trends	HDI
332	THERM	9	Evolution of Thermal Management in HDI	Russell, Jerry	Substrate Tech	HDI
333	MVIA	9	Implementing Microvia amd Flip Chip Technologies	McElroy, Jim	NEMI	HDI
334	TEST	9	Test Trends, How Electrical Test Requirements affect Design	Desai & Buetow	IBM IPC	PC
335	CAD	9	Forging Links in CAE, CAD, CAM Chain Requires New Methods	Small, Charles, H.	Comp Design	Con
336	BUS	9	FireWire Heats up the Action on VXI Bus	Desposito, Joseph		Elec

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337	SI	9	Elegant Yet Simple Tools Unmask Timing Flaws	Frederikson, Mark	IBM	EDN
338	CAD	9	PCB and MCM Design Tool Survey	ISD	ISD	ISD
339	EMI	9	Prepare Now for the Coming Onslaught of EMI Compliance Regs	Small, Charles, H.	Comp Design	Con
340	BUS	9	LVDS Invades bus, Board-level Applications	Small, Charles, H.	Comp Design	Con
341	BUS	9	Bus Analyzers Maximize PCI Performance	Staff	Comp Design	Con
342	SI	9	Integrated Simulation Technique Pinpoints SI Problems Up Front	Harrs Lin	AMP	Con
343	EMI	9	Unscrambling the European Power Directives	Lindman, Per	Ericsson	Elec
344	CAD	9	Printed Circuit Board Changes Enable New Design Possibilities	Ajluni, Cheryl		Elec
345	SI	9	Board Level Signal Integrity Analysys: Sooner is Better	Lipman, Jim	EDN	EDN
346	SI	9	Signal Integrity Analysis and Simulation Survey	EDN	EDN	EDN
347	BUS	9	3D Graphics Drive Speeding Buses	Biancomano, Vince	Comp Design	Con
348	FAB	9	Multiwire Today	Kunkle, Rob	I-Con	PC
349	DES	9	IPC-D-317A Design Guidelines for High Speed Packaging	IPC	IPC	IPC
350	FAB	9	IPC-DW-424 General Spec for Multiwire PCBs	IPC	IPC	IPC
351	FAB	9	PCB Pricing for 4,6 & 8 layer PCBs 1995	Ritchey, Lee W.	3Com	3Co
352	BUS	9	PCI Bus Goes Into Overdrive	Boyd-Meritt, Rick		EE
353	XMIS	9	All Stacked Up (Using 2D Field Solvers)	Bagatin, Eric etal	Ansoft	PC
354	FAB	9	Failure of Thick PCB Vias With Multiple Assembly Cycles	Knadle, etal	IBM	IBM
355	BGA	9	Mechanical Reliability and FA of PBGA Packages on Imm Ni/Au	Mei, Zequn etal	HP	HP
356	MVIA	9	Microvia Technology Advances PC Design Capabilities	Morehead, Mark	Arlon Corp	Wire
357	MATL	9	High Tg Materials Property Chart (Nelco)		Nelco	Nelc
358	BUS	9	LVDS Data Sheet from National		National	Nati
359	CAPS	9	Rewriting the Laws of Physics (Letter on bypass caps & Brooks)	Ritchey, Lee W.	3Com	PC
360	CAPS	9	Power-plane Resonance (Plane Capacitance & Fast Edges)	Johnson, Howard	Sigcon	EDN
361	EMI	9	Fight EMI by Modulating Your Clock Fequency	Leff, Barry J.	IC Works	Port
362	EMI	9	Intentional Clock Modulation for EMI Control	Johnson, Howard	Sigcon	EDN
363	DES	9	Gigabit Ethernet over Copper	Rao, Sailesh etal	Level One	Con
364	DES	9	A Quarter Wave Length Antenna with Superimposed Square Patc	Kossiavas, G etal	Univ de Nice	Mic
365	DES	9	High Speed PHY Design (for ENET)	Turudic, Andy	TriQuint	Con
366	EMI	9	EMC Measurement Procedures for ICS (SAE J1752)	SAE	SAE	SAE
367	CAD	9	GenCAM Procedure Description	IPC	IPC	IPC
368	MVIA	10	Cost Impacts of HDI, Cost of various Microvia Choices	Mike Buetow	HDI Express	IPC
369	CAD	10	Timing Analysis Tool Survey	Staff	ISD	ISD
370	CAD	10	Windows EDA Tools, Analysis Tools Ported to Windows	Staff	ISD	ISD
371	CAD	10	Windows EDA Tools: PCB & MCM Design	Staff	ISD	ISD
372	CAD	10	Windows EDDA Tools: Schematic Capture	Staff	ISD	ISD
373	CAD	10	Design Entry Tools	Staff	ISD	ISD

Article Number	TOPIC	BOOK	TITLE	AUTHOR	PUBLICATION	CC
374	CAD	10	HDL Simulators	Staff	ISD	ISD
375	THERM	10	TCAD Tools for Thermal Management	Lien, H.P. etal	Int Sys Eng	Adv
376	MATL	10	Thermal Interface Materials	Vogdes, Christine	Raychem	Adv
377	CAD	10	Packaging Design for High Performance ICs	Nunn, Wayne	VLSI	ISD
378	CAD	10	Analog and Mixed Signal Simulators: Focus Report	Bassak, Gil	ISD	ISD
379	CAD	10	Tools & Teamwork are Key to Successful PCB Design	Donlin, Mike	Comp Design	Cor
380	MVIA	10	Laser Microvia Drilling: Recent Advances	Schaeffer, Ronald		Circ
381	EMUL	10	The Hardware/Software Coverification Challenge	Tuck, Barbara	Staff	Cor
382	SI	10	Interconnect Synthesis Methodology,, Mentor Interconnectix	Doyle, Greg etal	Mentor	PC
383	CAD	10	Formal Verification Helps Stamp Out Design Bugs,	Ajluni, Cheryl	Elec Design	Elec
384	PKG	10	CSPs Continue to Grow, Summary of Package Types		Tessera	Adv
385	FAB	10	PCB Changes Enable New Design Possibilities	Aljuni, Cheryl	Elec Design	Elec
386	DES	10	Mentor Graphics, HP Eesof Team up to Upgrade RF Design Tool	Small, Charles, H.	Comp Design	Cor
387	SPEC	15	FiberChannel Disc Subsystem Spec. Seagate	Whittington, etal	Seagate	Sea
388	SPEC	BUS	SST_L BUS Spec. EIA/JESD8-8		EIA/JEDED	EIA
389	SPEC	BUS	PanelLink Bus SiI150 Silicon Images		SII	SII
390	SPEC	BUS	PanelLink DataSheets		SII	SII
391	BUS	10	Digital Buses, Analog Problems (Very good article, Rambus)	Strassberg, Dan	EDN	EDI
392	DES	10	Microprocessor Speed Table	?	?	?
393	DES	10	Good Wiring Leads to Accurate Measurements	Ferguson, Travis	Natl Instr	DE
394	SI	10	Models Make the Difference in High-Speed PC Board Design	Lipman, Jim	EDN	EDI
395	BUS	10	Armed for its Post-Adolescent Phase, Compact PCI Comes Age	Child, Jeff	Elec Design	Elec
396	DES	10	Probes Improve to Meet Speed and Space Challenges	Desposito, Joseph	Elec Design	Elec
397	XMIS	10	Skin Effect vs. Freq. Chart	?	?	?
398	XMIS	10	Transmission Line Scaling	Johnson, Howard	Sigcon	EDI
399	TEST	10	DFT Enhances PCB Manufacturing	Carlsson, Gunnar	Ericsson	FUT
400	FAB	10	The Use of Various Copper Protection Media	Barr, Gordon etal	Pagg	FUT
401	FAB	10	Area Array Packages and High-Density PWBs	Savolainen, Petri	Nokia	FUT
402	RES	10	Implementation of Buried Resistors on PCBs	Doeling, Wallace D	Sequent	FUT
403	CAPS	10	The Innovative SIMOV Technology Plane Capacitance	Bleiweib, Heinz	Seimens	FUT
404	PKG	10	integrated Circuit Package Development (good trends)	Hayward, James	AMD	FUT
405	MVIA	10	Microvias, Where Silicon and PCB Technology Meet	Lassen, Charles	Intel	FUT
406	TEST	10	Test Technology for MCMs, Chip Scale, Ceramic, etc.	Zimmerman, Karl L	CK Tech	FUT
407	BGA	10	Assembly and Interconnect Reliability if BGAs	Mawer, etal	Motorola	FUT
408	DES	10	GenCAM Addresses High Density Circuit Boards	Bergman, Deiter	IPC	FUT
409	BGA	10	Design & Process Optimization for 1 mm CCGA	Cole, etal	IBM	FUT
410	FAB	10	Alternate PCB Surface Finish Electrless TIN	Smetana, Joe	DSC	FUT

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411	BGA	10	Electroless Nickel-Gold Reliabilioty on BGAs	Cordes, Franz etal	AMKOR	FUT
412	MATL	10	Advanced Materials for Multilayer Technology	Fisher, Jack	ITRI	FUT
413	BUS	10	A Case for LVDS as the Umbiquitous Interconnect Technology	Goldie, etal	National Semi	Elec
414	BUS	10	Cooler Acceptance for the Firewire Bus?	Elphick, Mike	Elec Sys	Elec
415	DES	10	HDI Terms and Definitions		HDI Express	HDI
416	BGA	10	BGA Sockets	Wells CTI		EDN
417	DES	10	Smith Charts made easy	Schweber, Bill	EDN	EDN
418	DES	10	Strongarm on Steroids goes Intel Nod	PG	Port Desgn	Port
419	DES	10	New Mixed-Signal Tools System on a Chip SOC	Lipman, Jim	EDN	EDN
420	BUS	10	Line Drivers/Receivers Conform to New LVDS Standards	Staff	EDN	EDN
421	FAB	10	Acoustic Microimaging in Microelectronics	Oren, Kerry D.	ITT	FUT
422	CAD	10	Focus Report: Design for Test Tools	Aycinena, Peggy	ISD	ISD
423	DES	10	Board Level Programming using Emulation	Dugar, Vince	Storage Tech	Elec
424	DES	10	Assessing Haredwar/Software Codevelopement- Emulation	Bunza, Geofrrey	Synopsys	Elec
425	FAB	10	Through Hole Clearances- Plane clearances & Slots	Johnson, Howard	Sigcon	EDN
426	DES	10	Embedded Antennas Offer Potential For Reduced SAR, phones	McCartney, David	Range Star	Wire
427	MATL	10	FR-4 Dead as Dillinger?	Jorgensen, Chris	IPC	PC
428	DES	10	mils to mm conversion chart	Lee		
429	DES	10	Metric to English Conversion Chart	Lee		
430	MVIA	10	Chris Katzo Build UP Microvia PCB	Katzo, Chris	OPC	OPC
431	MVIA	10	PWB Circuit Manufacturability in Microvia & HighDensity	Gonzalez, etal	Dupont	Circ
432	RES	10	Electrical Test Techniques for Buried Resistors	Zengshu, etal	China	Circ
433	EMUL	10	Reconfigurable Prototyping Speeds Hardware/Software integratio	Dugar, etal	Storage Tech	ISD
434	CAPS	10	Low-k Means Reduced parasitc Capacitance	Havemann, Robt	TI	EE
435	EMI	10	90 Degree Corners, The Final Turn EMI- Reflections etc	Brooks, Doug	Unicad	PCE
436	FAB	10	Lead Free Solder, Amounts used in Industries	Prasad, Ray	Prasad Ent	SM
437	MVIA	10	Berefits of Hole Plugging for Micro Via PCBs	Albrecht etal	PPE	PPE
438	FAB	10	Beyond Gerber, The Birth and Growth of GenCAM	Bergman, Deiter	IPC	PC
439	DES	10	Digital Control for Model Railroads	Schweber, Bill	EDN	EDN
440	BUS	10	Rambus- Reality, Finally	Dipert, Brian	EDN	EDN
441	CAD	10	CAD/CAM Viewers	Sullivan, Kimberlee	PC Design	PC
442	FAB	10	Why GenCAM, Why now?	Bergman, Deiter	IPC	PC
443	CAD	10	CAD To CAM Exchanges	Church, Mike	Zuken Redac	PC
444	XMIS	10	Potholes, Xmission Line Defects size vs. Edge Rate	Johnson, Howard	Sigcon	EDN
445	EMI	10	Spread Spectrum EMI Reducing Methods & Parts	Cypress	Cypress	EDN
446	DES	10	Multiboard System Analysis	Kraemer, Doug	Viewlogic	PC
447	DES	10	Mechanical Analysis	Wellers, Fred etal	Pacific Numerix	PC

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448	SI	10	Spice or Ibis	Powell, Jon	Viewlogic	PC
449	EMUL	10	Chip Prototyping System up to 1.2 M Gates, Aptix	Aptix	Aptix	Wir
450	SI	10	Implementing an Internal Signal Integrity Department	Ritchey, Lee W etal	Speeding Edge	PC
451	CAD	11	How to Design Differntial Signalling Circuits	Ritchey, Lee W.	Speeding Edge	PC
452	DES	11	Examining Rules of Thumb, Right angles and Plane Cuts	Ritchey, Lee W.	Speeding Edge	PC
453	CAD	11	PCB Routers and Routing Methods	Ritchey, Lee W.	Speeding Edge	PC
454	MATL	11	Separating Science from Science Fiction, Materials Article	Ritchey, Lee W.	Speeding Edge	Circ
455	MATL	11	Who Cares About Tg?	Ritchey, Lee W.	Speeding Edge	Circ
456	MATL	11	New Printed Wiring Board Materials for GBEN AMP Study	Morgan, Etal	AMP	EDI
457	XMIS	11	PCB Interconnect Characterization From TDR Measurements	Smolyansky. Etal	TDA Sys	PC
458	XMIS	11	Terminating Differential Signals on PCBs	Crisafulli etal	Hyperlynx	PC
459	DES	11	The Power of Design Collaboration, Ambitech & Nexabit	Marconi etal	Nexabit	PC
460	SI	11	Signal Integrity Software, a Closed Loop Design Process SI	Kowal, Keith	Cabletron	PC
461	EMI	11	Silence is Golden, EMI Design Techniques, ENET	Dean, Dallas A.	Technitrol	PC
462	EMI	11	Noise Fighting 101, Spread Spectrum Clocking in Printers	Gardiner etal	Lexmark	PC
463	CONN	11	BetaPhase Connectors and Apple	Crum, S.	EPP	EPF
464	EMI	11	The Art of EMC, Using Quanitc Tools to Simulate	Wexler etal	Quantic Labs	PC
465	DES	11	Trace Widths vs. AWG Sizes and Resistivity	Jodoin, Claude	Self	PC
466	EMUL	11	Getting Physical, Virtually, Virtual Prototyping	Blomberg, Eric	Cadence	PC
467	FAB	11	For PCBs, The Finish is in Sight, HASL, AU/Ni, etc.	Buetow, Mike	IPC	PC
468	DES	11	Being First Matters, Virtual Protos and Cost of Time	Russell, Edmond	Thompson	PC
469	MVIA	11	The Via Squeeze, Nokia Cell Phone Build up	Lassen, etal	Nokia	IEE
470	CAD	11	Focus Report: PCB & MCM Tools	Bassak, Gil	ISD	ISD
471	DES	11	Ground Bounce Part 1 & 2 Brooks Speak	Brooks, Doug	UlriCad	PC
472	BUS	11	Direct Rambus Technology: The New Mainstream Standard	Crisp, Richard	Rambus	IEE
473	THERM	11	Thermal Modelling and Simulation of PCBs in CAD Integrated Flo	Wellers, Fred etal	Pacific Numerix	PC
474	CAD	11	Models for SI Simulation IBIS vs. Spice	Green, Lynnn	Hyperlynx	PC
475	BUS	11	LVDS Drivers Exceed 400 MB/S Pericom Parts	Pericom	Pericom	
476	XMIS	11	Differential Signalling, Measuring Differential Impedance	Johnson, Howard	Sigcon	EDI
477	EMI	11	Suppress EMI with Spread Spectrum Timing	Chen, Ian	Cypress	Por
478	MVIA	11	A Cost Analysis of Microvia Technologies	Singer etal	IBISS	PC
479	FAB	11	The GenCAM Format	Bergman, Deiter	IPC	PC
480	IMP	11	What is Characteristic Impedance (Good)	Bogatin, Eric	Bogatin Ent	PC
481	BUS	11	The Right Technique Yields Critical Rambus SI Measurements	Resso etal	HP	EDI
482	EMI	11	Selecting EMI Filtered Connectors	Sienicki, John	Spectrum Cont	EDI
483	CAD	11	1999 Buyer's Guide to CAD/CAM Tools	PC Design	PC Design	PC
484	CAD	11	Schematic, Layout and Autorouters, Some data Sheets	Sullivan, Kimberlee	PC Design	PC

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485	CAD	11	At $1000, Tool Broadens Access to EM Field Solvers	Clarke, Peter	EE Times	EE
486	MATL	11	Rogers RO 4003 & 4350 Specs	?	Microwave J	Mic
487	BUS	11	Fast Backplanes Ride New Gigabit Serial Interconnect	Wade, Will	EE Times	EE
488	BUS	11	Fairchild Tips High-Speed Backplane Plans at Designcon 2000	Ohr, Steven	EE Times	EE
489	BUS	11	3 GB Backplane Connection System from Thomas & Betts	Richter, Allan	EE Times	EE
490	CAD	11	Cadence Gains Sun's PCB Power PlaneAnalyser	Santarini, Mike	EE Times	EE
491	EMI	11	Clock Generator Chip Lets Designers Tune EMI	Day, John	EE Times	EE
492	RF	11	Bluetooth Definition		EE Times	EE
493	DES	11	ESR and Bypass Capacitor Self Resonant Behavior, Selecting CA	Brooks, Doug	UlriCad	Ultr
494	SI	11	Logic Life Cycle Curve from National		Elec Sys	Elec
495	FAB	11	Eclipse PCB Price Table		3Com	3Co
496	BUS	11	LVDS Output & Input Schematic & Voltage Levels	Schwartz, Milt	National Semi	Nati
497	BUS	11	Tranceiver Chip Replaces Parallel Backplanes- 1.25 GB LVDS	Desposito, Joseph	Elec Des	Elec
498	MVIA	11	The Truth About Microvias	Fitts, Mike	Solution Fitts	PC
499	CAD	11	High Speed Design's Ratchet Man, Lee Ritchey Feature	Goering, Richard	EE Times	EE
500	FAB	11	Anatomy of a Drilled Through Hole in a PCB	Ritchey, Lee W		
501	BGA	11	Chip Scale Packaging Choices and Challenges	Fjelstad, Joe		PC
502	DES	11	Using Routing Techniques to Minimze Skew	Horine, Bryce etal	Intel	Circ
503	FAB	11	GenCAM: Version 1.0	Bergman, Deiter	IPC	Circ
504	RES	11	Integral Resistors in High Frequency PCBs	Mahler, Bruce	Ohmega	Mic
505	MATL	11	Materials for High Speed Design	Hartley, Rick	Appl Inovat	PC
506	DES	11	Buried Capacitors in Various 3Com PCBs	Larsen, Jelena	3Com	3Co
507	DES	11	Bullet Power System Impedance vs. Frequency	Zasio	Packetcom	3Co
508	CAPS	11	Low Inductance Capacitors		Aerovox	Aer
509	CAPS	11	The Need for Low Inductance Capacitors	Galvagni etal	Aerovox	Aer
510	CAPS	11	Low Inductance Capacitors for Digital Circuits	Galvagni, John	Aerovox	Aer
511	DES	11	Decoupling Basics	Martin, Arch	Aerovox	Aer
512	CAPS	11	Improved Noise Suppression via Multilayer Caps in Power Entry	Martin, Arch	Aerovox	Aer
513	DES	11	Advanced Decoupling Using MLC Capacitors	Prymak, John	Aerovox	Aer
514	DES	11	Comparison of Metalization Technques for MFG of PCBs	Katzo, Chris	OPC	OP
515	DES	11	GLVDS by Ericsson		Ericsson	Eric
516	DES	12	An Introduction to High Speed Design	Ritchey, Lee W.	Maxtor	PC
517	PS	12	High-end Digital Systems Give a Thumbs Down to Rules of Thum	Greim, Michael	EDN	Mer
518	SI	12	Spice Provides Signal Integrity Clues for High-speed Systems	Boorom, Ken	EDN	HP
519	SI	12	Stop Taking Your Models for Granted	Ajluni, Cheryl	Staff	Elec
520	SI	12	The Nuts and Bolts of Signal Integrity Analysys	Haller, Robert	Compaq	EDN
521	XMIS	12	Differential Termination	Johnson, Howard	Sigcon	EDN

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522	PS	12	Power Distribution System Design Methodology for CMOS	Smith, Larry etal	SUN	IEE
523	XMIS	12	Analyze Transmission Lines with (Almost) no Math	Schmitt, Ron	Nortel	EDI
524	XMIS	12	Effects of Turning Vias on Bandwidth and Signal Quality	Ritchey, Lee W	Speeding Edge	
525	RF	12	RF & Microwave Basics	Reed, Dale	Trompeter	PC
526	FAB	12	Pulse Reverse Plating	Gutierrez, Enrique	TEchNu	Circ
527	FAB	12	Nickel and Gold Plating in Electronic Packaging	Lovie, John		EPF
528	FAB	12	Connectors: Choosing the Right Contact Materials	Mroczkowski, Rob	AMP	EPF
529	DES	12	Web Resources for Designers and Engineers	Staff	PC Design	PC
530	BIO	12	Profile of Lee Ritchey	Maisen, Mike	ISD	ISD
531	DES	12	XCITE Digital Controlled Z I/O	Alexander, Mark	Xilinx	Xlin
532	BGA	12	Comparison of Elect & Thermal Parameters of IC Packages	Huchzermeier, J	TI	TI
533	XMIS	12	Termination of ECL Logic Devices	Shockman, Paul	On Semi	On
534	CAD	12	Tools & Technologies, CAD Tool Survey	Staff	ISD	ISD
535	PS	12	Simultaneous Switch Noise and Power Plane Bounce CMOS	Smith, Larry etal	SUN	IEE
536	CAPS	12	ESR and ESL of Ceramic Capacitor Applied to Decoupling	Smith, Larry etal	SUN	IEE
537	CAPS	12	Decoupling Capacitor Calculations for CMOS Circuits	Smith, Larry etal	SUN	IEE
538	PS	12	Power Plane Spice Models for Freq & Time Domains	Smith, Larry etal	SUN	IEE
539	PS	12	Partitioning and Layout of a Mixed Signal PCB, Good, Planes	Ott, Henry		PC
540	EMI	12	Mike King's Absurd 20h Rule Treatment	King, Mike		
541	PS	12	SF State Radiation Edge Effects in PCBs (20h rule look)	Pantic-Tanner, Z	SF State	SF
542	PS	12	Effects of 20-H Rule and Shielding Vias on EMI in PCBs	Chen, Huabo etal	UC SC	UC
543	XMIS	12	What Makes a Circuit "Hihg-Speed"?	Ritchey, Lee W	Speeding Edge	Futu
544	CAD	12	Floor Planners, The Centerpiece of Virtual Prototyping	Ritchey, Lee W	Speeding Edge	PC
545	BUS	12	Busses: What are They and How Do They Work?	Ritchey, Lee W	Speeding Edge	PC
546	BGA	12	The Effect of BGA Hole Patterns in Power Planes on High Speed	Ritchey, Lee W	Speeding Edge	Tec
547	XMIS	12	Design Considerations for Gigabit Backplane Systems	Cohen, Tom etal	Teradyne	Des
548	MVIA	12	How Reliable are Microvia PCBs?	Trefzer, Jurgen etal	PPE	Circ
549	XMIS	12	Use TDR for Disc-drive Flexible Interconnect Characterization	Smolyansky. Etal	TDA Sys	EDI
550	DES	12	Useful Acronyms	Staff	EDN	EDI
551	MATL	13	Halogen Free PCB Materials	Valfridsson, Martin	Ericsson	Circ
552	FAB	13	Non-contact Electrical Test of PCBs	Odan, Yuji etal	OHT	Circ
553	BGA	13	TI BGA Packages for TTL Parts	AD	EE Times	EE
554	FAB	13	Guide to Lead Free Soldering	Staff	SMT	SM
555	DES	13	Predictive Engineering- PCB Design Framework	Holden, Happy		Circ
556	MATL	13	Living in a Material World- Need for High Frequency Matls	Aguayo, Art	Rogers	PC
557	BGA	13	Packaging Solves the Last Centimeter	Israelsohn, Joshua	EDN	EDI
558	PS	13	Optimize Power Distribution Analysis in High-Speed Designs	Westerhoff, Todd	Cadence	Elec

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559	FAB	13	Lead-Free Solder: the Sn/Ag/Bi System	Hwang, Jennie	H-Tech	SM
560	CAD	13	CAD/CAM Viewers- listing of products	Sullivan, Kimberlee	??	PC
561	DES	13	Process Refinement- Data toMfg	Bondi, Mike etal	Celestica	PC
562	MATL	13	Nonwoven Laminates-	Funer, Rolf	Hadco	Circ
563	BGA	13	Designing with CBGAs- Reliability Analysis	Becker, Mike etal	BCPL	SM
564	BGA	13	Column Grid Array- Hi Rel Option for Packaging	Strucken, Keith	Lockheed- Mar	ADV
565	CAPS	13	Parasitic Inductance of a Bypass Capacitor	Johnson, Howard	Sigcon	EDN
566	BGA	13	High-Performance Laminated Chip Package Technology	Petefish, William eta	Gore	HDI
567	MATL	13	Nonwoven Laminates and Prepregs in HDI PWBs	Khan, Subhotosh	DuPont	HDI
568	DES	13	Who's Afraind of the Big,Bad Bend? Right Angle Turns	Johnson, Howard	Sigcon	EDN
569	DES	13	Proper Grounding is Critical For High-Speed Systems	Kester, Walt etal	Analog Devices	Wir
570	SI	13	The Ramifications of Component Selection, lead Inductance	Bogatin, Eric	Gigatest	PC
571	IMP	13	Accurate Measurements on High-Speed Rambus Traces	Resso, Mike etal	Agilent	Elec
572	CAD	13	PCB Design Tools- A Survey of Tools	Maisen, Mike	ISD	ISD
573	DES	13	Serpentine Delays	Johnson, Howard	Sigcon	EDN
574	XMIS	13	50 Ohm Mail Bag, Why 50 Ohms?	Johnson, Howard	Sigcon	EDN
575	CONN	13	Gold vs. Tin onConnector Contacts	Whitley, J. H.	AMP	AMI
576	CONN	13	Connector Reliability Considerations	Byrne, Joe	Memorex	Mer
577	CONN	13	Fretting Corrosion in Electrical Contacts	Bock, E. M. etal	AMP	AMI
578	XMIS	13	Differential Signalling Cuts Noise, Distortion, and Interference	Checkovich, etal	Analog Devices	Elec
579	EMI	13	System-Clock IC Lets You Program Spectrum for EMI	Schweber, Bill	Int Micro Ckts	EDN
580	FAB	13	The Top PCB Shops	Nakahara, Hayao	N.T. Info	PC
581	BGA	13	BGA Tensile Testing with Alternative PCB Finishes- Part 1	Houghton, Bruce	Celestica	PC
582	DES	13	Anatomy of a Plated Thorugh Hole	Ritchey, Lee W.	Speeding Edge	Spe
583	PS	13	Don't Cut Your Ground Planes E-mail Report	??	??	E-m
584	PS	13	Syncor PS Specs	??	Syncor	Syn
585	SI	13	Design Con Paper Web Sites	Dambrosia, John	Tyco	E-m
586	CAPS	13	Upper Limit on Interplane Capacitance, resonances	Smith, Larry etal	SUN	SUN
587	XMIS	13	90 Degree Bend Models	??	??	??
588	RF	13	Partitioning for RF Design	Kowalewski, Andy	NEC	PC
589	EMI	13	Ferrite Beads	Johnson, Howard	Sigcon	EDN
590	MATL	13	A Substrate for All Seasons- All Matls	Kuszaj, Mike etal	Rogers	PC
591	FAB	14	Lead-Free Solders and Their Properties	Prasad, Ray	Consultant	SM
592	DES	14	Effect of BGA Hole Patterns in Power Planes on High Speed	Ritchey, Lee W.	Speeding Edge	Tec
593	FAB	14	Technology Road Map Fab Dimensions		Multek	Mul
594	FAB	14	The PCB Industry Then and Now	Ritchey, Lee W.	Speeding Edge	PC
595	BUS	14	LVDS Electrical Operation- Schematic		National Semi	

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596	DES	14	Getting a Hold on Hot-Swap Hardware	Davis, Henry	Consultant	CSI
597	EMI	14	Understanding Electromagnetic Fields and Antenna Radiation	Schmitt, Ron	Sensor Res	EDI
598	BGA	14	TAB Excels in Fine-Pitch Applications	Markstein, Howard	Staff	EPF
599	EMI	14	Noise Fighting Components	Brooks, Doug	UltraCAD	PC
600	BGA	14	A Chip-Scale PackagePrimer	Malatesta, Jim etal	Intel	PC
601	MATL	14	Trends in Electronic Substrate Technology	Senese, Tony	Nelco	EPF
602	CONN	14	Revolutionary High Performance Interconnect Max density	Patel, Guatam etal	Teradyne	Tera
603	XMIS	14	Using Creative Silicon Technology to Extend BP to 3.125 GB/S	Galloway, Paul etal	Velio	Veli
604	EMI	14	Practical Analysis and Characterization of Lossy Xmission Lines	Bogatin, Eric	Gigatest	PC
605	FAB	14	BGA Tensile Testing with Alternative PCB Finishes Part 2	Houghton, Bruce	Celestica	PC
606	XMIS	14	Signal Integrity Considerations for HS Data Xmission in a PCB	Cohen, Tom etal	Teradyne	Tera
607	MVIA	14	Microvia Capability, Quality and the Impact of Registration	Rhodes, Ray	CAY	Circ
608	BUS	14	BLVDS Takes Care of Most Connections	Chang, James	National Semi	EE
609	BUS	14	Taking The Measure of Gbit-plus Buses	Kraus, Robert	Inova Semi	EE
610	BUS	14	Interconnecting Common Interfaces PECL to CML	Reese, Jacob etal	Maxim	EE
611	SI	14	Signal Integrity Analysis Reaps Huge Dividends for Network PCB	Pichlmaler, Hans, et	Siemens	ISD
612	SI	14	Strange Microstrip Modes	Johnson, Howard	Sigcon	EDI
613	XMIS	14	Controlled Impedance PCBs	Polar Inst	Polar Inst	Pola
614	SPEC	14	HSTL Buffer Spec EIA/JESD8-6	EIA	EIA	EIA
615	XMIS	14	Gigabit Backplane Design, Simulaton & Measurement	Patel, Guatam etal	Mixed Cos	Des
616	XMIS	14	Signal Integrity Considerations for 10 Gbps Xmission in Backplan	Patel, Guatam etal	Teradyne	Des
617	XMIS	14	GTLP in Live Insertion Applications	Cox, ernest, etal	TI	Des
618	BUS	14	Compact PCI at 66 MHz	Unk	Unk	Des
619	XMIS	14	Optical Backplanes- Fantasy or Reality?	Murphy, Beth etal	AMP	AMI
620	XMIS	14	Evaluation of Maximum Usable Lengths for Cabled Copper Interc	Fogg, Michael	AMP	Des
621	BGA	14	BGA Termination Alternatives	Mahler, Bruce	Ohmega	EPF
622	DES	14	Power Plane Thermal Tie Design	Ritchey, Lee W.	Speeding Edge	Spe
623	CAPS	14	Analytical & Experimental Analysis of Cap/Plane Interactions	Fallah, Ahmad etal	Cienna	Cier
624	XMIS	14	Design Considerations for Gigabit Backplane Systems PPT Slides	Patel, Guatam etal	Teradyne	Des
625	XMIS	14	The Impact of PWB Construction on High-Speed Signals	Morgan, Chad, etal	AMP	Des
626	XMIS	14	Practical Guidelines for Implementing 5 Gbps in Copper to 10 Gb	Rothermel, Brent eta	AMP	Des
627	SPEC	15	SSTL_2 Stub Series Terminated Logic 2.5V EIA/JESD8-9	EIA	EIA	EIA
628	SPEC	15	Mil Spec 55110-D	US Army	ERDA	
629	SPEC	15	Mil Std 275E Printed Wiring for Electronic Equipment	DOD	DOD	DOI
630	SPEC	15	Mil P 50884B Printed Wiring, Flex and Rigid Flex	DESC	DESC	DES
631	SPEC	15	IPC-D-317 Design Guidelines for High Speed Circuits	IPC	IPC	IPC
632	SPEC	15	IPC-2141 Controlled Impedance Circuit Boards & High Speed	IPC	IPC	IPC

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633	SPEC	15	RS-232-E EIA/TIA-232-E Bus Spec	EIA	EIA	EIA
634	SPEC	15	IPC-T-50 Terms and Definitions	IPC	IPC	IPC
635	SPEC	15	IPC-D-316 Design Guideline for Microeave PCBs	IPC	IPC	IPC
636	CONN	16	Teradyne GbX Connector Paper	Cartier etal	Teradyne	Tera
637	FAB	16	Data Circuits Laminate Info Sheet	Data Circuits	Data Circuits	Dat
638	CAPS	16	Decoupling Capacitance, Theory and Applications	Hubing, Todd etal	UMR	UMI
639	CAPS	16	Power Bus Ripple & Radiated EMI Tests	Grasso, Charles	StorageTek	Stor
640	PS	16	ADC Grounding	Johnson, Howard	Sigcon	EDN
641	REL	16	Minimizing Failures on Electronic Systems by Design	Lakshminarayanam	India	EDN
642	XMIS	16	What Makes a Circuit High Speed?	Ritchey, Lee W.	Speeding Edge	Boa
643	SI	16	IBIS Evolves	Powell etal	Viewlogic	PC
644	CAD	16	Power Analysis Tools Survey	Staff	ISD	ISD
645	CAD	16	Timing Analysis Tools Survey	Staff	ISD	ISD
646	CAD	16	PCB Design Tools Survey	Staff	ISD	ISD
647	SI	16	Why You Need to Start Thinking About Signal Integrity Now!	Strange, Rod	SiQual	Elec
648	RF	16	The Frequency Domain: A Whole Nother Way of Thinking	Strassberg, Dan	EDN	EDN
649	SI	16	Developing Simulation Models for High-Speed Applications	Mu, Zhen etal	Pacific Numer	PC
650	BUS	16	The Bus Protocol Stops Here	Ritchey, Lee W.	Speeding Edge	PC
651	XMIS	16	Both-ends Termination	Johnson, Howard	Sigcon	EDN
652	BGA	16	Roadmap to BGA Standards	Bergman, Deter	IPC	SM
653	SI	16	Signal Integrity Analysis	Levy, Yoram	Transelectric	PC
654	CAD	16	Routing the Path from Physical to Electrical Rules	Vaughn, Darrell	RouTech	PC
655	BIO	16	Designing on The Edge, Bio on Lee Ritchey	Shaughnessy, A	PC Design	PC
656	CAD	16	The Evolution of Manufacturing Output Formats	Morrison, Joe	ADIVA	PC
657	MATL	16	Is FR-4 Running out of Gas?	Jorgenson, Chris	IPC	PC
658	SI	16	Solution Space Analysis for High-Speed Design, up front SI Anal	Westerhoff, Todd	Cadence	PC
659	CAPS	16	Bypassing PC Boards: Thumb Your Nose at Rules of Thumb	Pattavina, Jeffrey	Intraplex	EDN
660	EMI	16	Meeting International Emissions Standards, Painlessly	Fenical, Jerry	Inst Spec	Port
661	SI	16	IBIS and SPICE Revisited, Can IBIS keep up with demands?	Powell, Jon	Viewlogic	PC
662	DES	16	Designing Electronic Equipment for ESD Immunity	Barnes, John	Lexmark	PC
663	MFG	16	The Ramifications of Component Selection	Bogatin, Eric	Gigatest	PC
664	CAD	16	Design Archiving	Staples, Vaughn	Intercept Tech	PC
665	PS	16	Partitioning and Layout of a Mixed-Signal PCB	Ott, Henry	Ott Consulting	PC
666	PS	16	High-end Digital Systems Give a Thumbs Down to Rules of Thum	Greim, Michael	Mercury Comp	EDN
667	DES	16	Shared Resources Design Flow Chart	Ritchey, Lee W.	Shared Resourc	Sha
668	SI	16	Time and Frequency Domain Analysis of Right Angle Corners	Montrose, Mark	Montrose	Mor
669	FAB	16	Trace Resistance Equation from Ambitech	Stevens, John	Ambitech	Aml

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670	XMIS	16	Time Domain Reflectometry Theory	Agilent	Agilent	Agil
671	SI	16	Packhard-Hughes Connector Characteristics		Gigatest	Gig
672	MVIA	16	Forming Microvias	Bergman, David	IPC	PC
673	MATL	16	Implementation of High-Frequency Laminates	Jamsa, Markku	Aspocomp	PC
674	MATL	16	Trends in PCB Materials	Trobough, Doug	Merix	PC
675	FAB	16	Electroless Nickel/Immersion Gold and Black Pad	Walsh, Mike	OMG Fidelity	Circ
676	DES	16	Demystifying Component Slelction	Ritchey, etal	Speeding Edge	PC
677	PS	16	PWB Power Structures: Theory and Design	Hubing, Todd etal	UMR	UMI
678	EMI	16	EMI Guidlelines from Intel for USB	Intel	Intel	Inte
679	MATL	16	Material Simulations and Measurements from Multek Germany	Multek	Multek	Mul
680	DES	16	Floorplanning: The Centerpiece of Virtual Prototyping	Ritchey, Lee W.	Speeding Edge	PC
681	MATL	16	Designing for Imbedded Passives	Borland, William	Dupont	PC
682	FAB	16	Lead-Free Technology and Alloy Selection- Paart II	Huang, Jennie	H-Tech	Ind
683	XMIS	16	Modelling Skin Effect	Johnson, Howard	Sigcon	EDN
684	CONN	16	Connectors: Choosing the Right Contact Materials	Mroczkowski, Rob	AMP	EPF
685	MVIA	16	How Reliable are MicroVias?	Trefzer, etal	PPE	Circ
686	CAD	16	Document and Data Deliverables for Product Data Transfer	Borinski, etal	3Com	3Cc
687	CAPS	16	Power Bus Noise Reduction using Power Islands in PCBs	Hubing, Todd etal	UMR	UMI
688	DES	16	Examination of NextLev Connector Patterns	Ritchey, Lee W.	Speeding Edge	Spe
689	XMIS	16	High Speed Serial Link Board Level Considerations	Mantiply, Paul	Procket	Pro
690	XMIS	16	Vdd_HSSL Bypass Measurements	Frasier, Arthur	Procket	Pro
691	BGA	16	58 mm Package Simultaneous Switching Noise Simulations	Argyrakis, Straty	Procket	Pro
692	BGA	16	58 mm/20 Layer Simulataneous Switching Noise Simulations	Argyrakis, Straty	Procket	Pro
693	XMIS	16	HSSL CPI-b0 Measurements	Mantiply, Paul	Procket	Pro
694	XMIS	17	Leaving "Ground" return current discussion	Bogatin, Eric	Gigatest	PC
695	MVIA	17	Cost-Effective Use of Microvias	Capers, Charles	Design Solution	PC
696	XMIS	17	Sounding Off on the "db"	Bogatin, Eric	Gigatest	PC
697	REL	17	Embedding Resistors and Capacitors	Funer, Rolf	Funer Assoc	PC
698	XMIS	17	The Return Current in a Transmission Line	Bogatin, Eric	Gigatest	PC
699	CAPS	17	The Impedance of a Real Capacitor	Bogatin, Eric	Gigatest	PC
700	XMIS	17	Lossy Line Simulation and Analysis	Smolyansky. Dima	TDA Sys	PC
701	FLEX	17	Stacked Flex Circuits	Solberg, Vern	Tessera	PC
702	CAD	17	The Cost of Poor Library Management	Shumpert, etal	Intel	PC
703	FAB	17	Designing for Fabricator Independence	Versiackas, Bob	Pronto Ckts	PC
704	CAD	17	The Importance of Design Data Management	Heidorn, Mark	Mentor Graphics	PC
705	XMIS	17	Get Your S (Parameters) Together	Bogatin, Eric	Gigatest	PC
706	FAB	17	Surface Finishes, and OEM Perspective	Barbetta, Mike	Cisco	Circ

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707	FAB	17	PTFE-Based Composites fir High Speed Digital Designs	McCarthy, etal	Taconic	PC
708	XMIS	17	Crossing Boundaries with High-Speed Data	Wong, Jim	National Semi	Net
709	FAB	17	Current and Conductors (Looks at old charts)	Jouppi, Michael	Thermal Man	PC
710	BUS	17	Interfacing LVDS With Other Differential I/O Types	Ju, Jeff	Fairchild	EDI
711	DES	17	Circuit Board Desing for 10 Gbit Optical Modules	Williams, Lawrence	Ansoft	EDI
712	FAB	17	Going Beneath the Surface of Surface Finished	Cullen, Don	MacDermind	Circ
713	XMIS	17	When to Worry About Lossy Lines	Bogatin, Eric	Gigatest	PC
714	XMIS	17	High Speed Tranmsission Line Requirements	Pochareddy etal	Ciena	Circ
715	des	17	Right the First Time PCB Design Flow for Net List Accuracy	Ritchey, Lee W.	Speeding Edge	Spe
716	PS	17	Low Impedance Power Delivery Over Board Frequencies	Fang, etal	Sigrity	PC
717	SPEC	17	X2Y Capacitor Data Sheets		Phicomp	Phi
718	DES	17	Right the First Time Book Review	Blyler, John	Wireless Sys	Wir
719	BUS	17	Piecing It Together, The Old & New in Backplanes & Buses	Wong, William	Elect Design	Ele
720	BUS	17	What a Difference a Signal Makes, Diff Signal Tutortial	Ritchey, Lee	Speeding Edge	Spe
721	BGA	17	Vcc and Ground Bounce Studies Virtex II 1152 BGA Package	Ritchey, Lee	Speeding Edge	Spe
722	BGA	17	Package Desing for High Performance Ics	Nunn, Wayne	VLSI	EE
723	XMIS	17	What You Loose From a Lossy Line	Bogatin & Garat	Gigatest	EDI
724	PS	17	Multiple ADC Grounding	??	EDN	EDI
725	FAB	17	Working With Fabricators, Tricks of the Trade	Breglio, etal	Adv Ckts	PC
726	MVIA	17	Assembly Issues with Microvia technologies (Good)	Ladhar etal	Solectron	SM
727	FAB	17	Build UP Fab Drawing with Microvias	??	Symbol	??
728	FAB	17	Should Nonfunctional Pads Be Removed From AW?	Ritchey, Lee W	Speeding Edge	Spe
729	XMIS	17	On Chip Bypassing With End Termination	Johnson, Howard	Sigcon	EDI
730	FAB	17	How Many Thermal Ties Are Needed To Connect Power Pins?	Ritchey, Lee W	Speeding Edge	Spe
731	SPEC	17	Procket Atlas Router	Procket	Procket	Pro
732	EMI	17	Picket Fences, Mike King Rambling			Sig
733	CAPS	17	Frequency Dependent Characteristics of Bulk & Ceramic Caps	Novak, etal	Sun	SUI
734	BGA	17	Simultaneous Switching Noise and Signal Integrity	Actel	Actel	Act
735	MATL	17	The History of Embedded Distributed Capacitance	Pfeiffer, Jole	3M	PC
736	XMIS	17	Maximizing 10Gbps Xmission Paths in Cu Backplanes	Clink, James	Winchester	Des
737	XMIS	17	Design at the Speed of 6 GB/S	Hartley, Rick	L-3 Com	PC
738	FAB	17	Analysis of Merix Sample PCBs Immer Ag vs Ni/Au	Zasio, John J	Caspian	Cas
739	XMIS	17	Backplane Via Pin Test PCB Design Spec	Mantiply, Paul	Procket	Pro
740	DES	17	Component Selection From the EE's View Point	Ritchey, Lee W	Speeding Edge	PC
741	MATL	17	Loss Tangent Comparison, Nelco 4000-13SI vs. Isola IS620	Ritchey, Lee W.	Procket	Pro
742	PS	18	Power System Voltage Distribution Considerations	Kapfer, Thomas	Kapfer Group	Kap
743	EMI	18	Radiated Emissions and Immunity of Microstrips	Hill,David etal	NBS	IEE

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744	PS	18	Measuring MilliOHms and PicoHenries in Power Distribution	Novak, Istvan	Sun	Des
745	PS	18	Power System Tests	Ritchey, Lee W	Speeding Edge	Spe
746	MATL	18	Woven Glass Reinforcement Patterns	Brist, Gary etal	Intel	PC
747	MATL	18	Best Materials for 3-6 GHz Design	Leys, Doug	Nelco	PC
748	MATL	18	Conductive Anodic Filaments (CAF)	Karavakis, etal	Nelco	Circ
749	FAB	18	PCBs: Fabricating the Truth	Ritchey, Lee W	Speeding Edge	Circ
750	EMI	18	Atlas P1 Proto EMI 2 & Conducted Results	Turcotte, Michael	Procket	Pro
751	XMIS	18	NX7 Test PCB Test Report	Ritchey, etal	Speeding Edge	Spe
752	XMIS	18	Serial Link Analysis for Mahi Networks	Ritchey, Lee W	Speeding Edge	Spe
753	SI	18	ADS Simulation of Very High Speed Nets	Cubillo, Romen	Mahi Networks	Mal
754	XMIS	18	Impedance Modelling on Multiple Dielectric Builds (good)	Gaudin, etal	Circuit World	Pol
755	PS	18	Spectrum Analyzer Plot Instructions	Zasio, John J	Caspian	Cas
756	BGA	18	Xilinx XC2V6000 FF1152 Signal Noise vs. IBM SuperBGA	Zasio, John J	Caspian	Cas
757	MATL	18	Embedded Capacitance Material Spec		3M	3M
758	XMIS	18	Serdes BackplaneExperiments, Shows Overdrive Effects	Werner, etal	AMP	TYC
759	SPEC	18	PCI Express Base Specification Rev 1		PCISIG	PCI
760	SPEC	18	RS485, RS422, RS232 & RS423 Quick Reference	Smith, R. E.	RS485.com	RS4
761	SPEC	18	Processor Speed, Complexity Chart	?	?	?
762	XMIS	18	Test Board Via Transition Analysis Report	Argyrakis, Straty	Procket	Pro
763	XMIS	18	Designing Equalizers for High Speed Copper Links		DesignCon03	Max
764	FAB	18	Selecting PCB Suppliers	Ritchey, Lee W.	Speeding Edge	Spe
765	MATL	18	Dielectric Spacing Calculations for Isola IS620		Isola	Isol
766	FAB	18	Drill Aspect Ratio Chart from Winonics		Winonics	Win
767	FAB	18	Sample Drill Table	Gunderson, Sage	Fabric7	Fab
768	PS	18	Zasio's PCB Probe Setup Photo	Zasio, John J	Caspian	Cas
769	PS	18	Decoupling Hi Speed with Embedded Capacitance	Peiffer, Joel	3M	3M
770	FAB	18	Cost Effective Backdrilling of Backplanes	Camerlo etal	Cisco	Circ
771	DES	19	TTL: Too Dated for Speedy Design	Ritchey, Lee W.	Speeding Edge	EE
772	DES	19	App Notes Not a Necessary Evil	Ritchey, Lee W.	Speeding Edge	EE
773	DES	19	Not All Fabricators Are Equal	Ritchey, Lee W.	Speeding Edge	EE
774	DES	19	Trade Offs of High Speed Design	Ritchey, Lee W.	Speeding Edge	EE
775	DES	19	DAC Lack: No Talk on Package Defects	Ritchey, Lee W.	Speeding Edge	EE
776	BGA	19	Inside FPGA Package Problems	Ritchey, Lee W.	Speeding Edge	EE
777	BGA	19	Fixing FPGA Package Problems	Ritchey, Lee W.	Speeding Edge	EE
778	BGA	19	Let's Get Right With Parts Info	Ritchey, Lee W.	Speeding Edge	EE
779	BGA	19	Readers Weigh in on Package Woes	Ritchey, Lee W.	Speeding Edge	EE
780	DES	19	Memory Interface Package Woes	Ritchey, Lee W.	Speeding Edge	EE

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781	BGA	19	The Cost of FPGA Package Defects	Ritchey, Lee W.	Speeding Edge	EE
782	DES	19	Current Source Volume 1	Ritchey/Knack	Speeding Edge	Spe
783	DES	19	Current Source Volume 2	Ritchey/Knack	Speeding Edge	Spe
784	FAB	19	The Search For The Universal PCB Finish	Barbetta, Mike	Cisco	PC
785	XMIS	19	A High Bandwidth Probing Plan	Bogatin, Eric	Synergetics	PC
786	XMIS	19	Probing For The Truth	Strassberg, Dan	EDN	ESI
787	MATL	19	Base Materials for High Speed, High Frequency PC Boards	Hartley, Rick	Applied Innovati	PC
788	XMIS	19	A Tutorial on HighSpeed Interfaces in the Telcom Market	Wong, Jim	National Semi	Nati
789	CAD	19	Allegro Color Layers for PCB Design	Gunderson, Sage	Fabric7	Fab
790	CAD	19	Artwork Layers, Minimum Suggested	Gunderson, Sage	Fabric7	Fab
791	XMIS	19	Feasibility of 3.125 GB/S in CMOS	Jenkins, Mike	LSI Logic	LSI
792	FAB	19	Fabrication Notes for Hi Tg FR-4	Ritchey, Lee W.	Speeding Edge	Spe
793	MATL	19	Thermoplastic Properties of Plain Weave Composites, Good	Brown, Eric etal	Univ of Ill	Uni
794	XMIS	19	Probing and Shielding Issues for Multi-Gigabit Signals	Smith, Doug	Doug Smith	Dou
795	SPEC	19	IBM Unilink Specifications		IBM	IBM
796	DES	19	Short Tutorial on Hi Speed for Int. Wafer Level Conf.	Ritchey, Lee W.	Speeding Edge	Spe
797	DES	19	Where Have we Been, Where Are We Going PWRPT	Ritchey, Lee W.	Mentor Users	Spe
798	MVIA	19	Microvia Design Guide (Shows Dimensioning)	?	Hadco	Had
799	XMIS	19	Turning Via and Compensation Trace ADS Simulation	Shih, Porsh	Procket	Pro
800	XMIS	19	Diff Pair Coupling Study	Ritchey, Lee W.	Speeding Edge	Spe
801	XMIS	19	Edge vs. Frequency Study, FFT of Switching Waveforms	Ritchey, Lee W.	Speeding Edge	Spe
802	DES	19	Technology Table Description	Ritchey, Lee W.	Speeding Edge	Spe
803	MATL	19	Material Evidence, A Tutorial on PCB Materials	Ritchey, Lee W.	Speeding Edge	Spe
804	FAB	19	Considerations When Designing a Stackup for a Multilayer PCB	Ritchey, Lee W.	Speeding Edge	Spe
805	FAB	19	Test Structures Needed for Multilayer PCBs	Ritchey, Lee W.	Speeding Edge	Spe
806	CAPS	19	Where Should Decoupling Capacitors be Placed?	Ritchey, Lee W.	Speeding Edge	Spe
807	CAPS	19	Should a Low Loss or High Loss Bypass Capacitor be Used?	Ritchey, Lee W.	Speeding Edge	Spe
808	FAB	19	General Specification for Printed Circuit Fabrication	Ritchey, Lee W.	Speeding Edge	Spe
809	XMIS	20	Xilinx Rocket I/O TransceiverCharacterization, Mahi	Valtenbergs, Sam	Mahi Networks	Mah
810	XMIS	20	Mahi Skin Effect and Dielectric Loss for 30 paths	Corley, Chuck	Mahi Networks	Mah
811	SPEC	20	Agere Systems Quad Serdes Specification		Agere	Age
812	DES	20	Current Source Volume 3	Ritchey/Knack	Speeding Edge	Spe
813	XMIS	20	How Do Return Currents Find Their Way From Plane to Plane?	Ritchey/Knack	Speeding Edge	Spe
814	XMIS	20	Test Resutls, High Speed Test PCB	Ritchey/Mantiply	Procket	Pro
815	FAB	20	Pad Stack Design and Power Plane Design	Ritchey, Lee W.	Speeding Edge	Spe
816	XMIS	20	Do Vias Act as Stubs?	Ritchey, Lee W.	Speeding Edge	Spe
817	FAB	20	What is Back Drilling?	Ritchey, Lee W.	Speeding Edge	Spe

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818	DES	20	A Challenge for IC Manufactuers	Ritchey, Lee W.	Speeding Edge	Spe
819	CAPS	20	What Size Capacitor Packages Should I Choose?	Ritchey, Lee W.	Speeding Edge	Spe
820	EMI	20	What is EMI and Wher Does It Come From?	Ritchey, Lee W.	Speeding Edge	Spe
821	CAPS	20	AVX Dielectric Comparison Chart	AVX	AVX	AV)
822	CAPS	20	AVX Intro to Choosing MLC Decoupling Capacitors	Chase, Yun	AVX	AV)
823	CAPS	20	Multilayer Ceramic Capacitors- Materials and Manufacture	Kahn, Manfried	AVX	AV)
824	CAPS	20	Y5V Capacitance vs. Voltage	NIC Comp	NIC Comp	NIC
825	CAPS	20	What Type of Insualtion Material Should I Use for Decoupling Cap	Ritchey, Lee W.	Speeding Edge	Spe
826	CAPS	20	What do EIA Numbers on Capacitors Mean?	Kemet	Kemet	Ken
827	XMIS	20	Cross Talk Study at Procket	Ritchey, Lee W.	Procket	Pro
828	FAB	20	The Electroless Copper Process	Clark, Raymond	PC Fab	SJ (
829	DES	20	Design Check List at Finnigan	Ritchey, Lee W.	Finnigan	Finr
830	REL	20	Reliability, an IEEE Spectrum Compendium	Various Authors		IEE
831	DES	20	Old TI Transistor Data Sheets	TI	TI	TI
832	EMI	20	Backplane EMI Filter Design and Test	Major, Don	Procket	Pro
833	DES	20	Difference Between Scientist and Engineer	Villani, D	??	??
834	DES	20	Joan Fan Letter On Design Success	Fan, Joan	SBE	SBE
835	FAB	20	The Quest For the Ultimate Surface Finish	Beauvillier, Luc	Merix	PC
836	MATL	20	The Impact of Material Selection	Hartley, Rick	Applied Innovati	PC
837	MATL	20	Thin PCB Lamiantes	Grebenkemper, Joh	Compaq	PC
838	FAB	20	Stackups for Procket PCBs 24 Layer	Ritchey, Lee W.	Procket	Pro
839	DES	20	Graphic Symbols For Electronic Components	Electronics	Electronics	Elec
840	DES	20	Signetics Linera Circuit Data Sheets	Signetics	Signetics	Sigr
841	DES	20	Signetics Utilogic Data Sheets	Signetics	Signetics	Sigr
842	CAPS	20	Kemet Ceramic Chip Capacitors- Good Description	Kemet	Kemet	Ken
843	XMIS	21	How Signals Are Degraded When Speeds Go Up	Ritchey, Lee	Speeding Edge	Spe
844	BGA	21	Xilinx 1152 Pin BGA Package AW	Xilinx	Xilinx	Xilir
845	FAB	21	The Effects of Lead Free on PCB Fabrication	McGrath, Bob	Teradyne	PC
846	XMIS	21	When Should I Worry About Lossy Lines	Bogatin, Eric	Bogatin Ent	PC
847	EMI	21	Effects of Ground Guard Fence on EMI	Lee, Heesok, etal	Korean Inst	IEE
848	TEST	21	PCB Design for Testability with Boundry Scan, etc.	Negron, Hector	Mahi Networks	Mal
849	FAB	21	Cray Buried Resistor Picture		Cray Research	
850	FAB	21	Pictures of Plated Through Holes		Electrochemicals	
851	XMIS	21	A Designer's Survival Guide to High Speed Serial Links	Bogatin, Eric	Bogatin Ent	PC
852	FAB	21	Incoming Inspection Procedure for High Speed PCBs	Lee, Sherman	Procket	Pro
853	FAB	21	Plated and Filled Via-in Pad, and Other Via Capping Methods	Stephens, John	Merix	Mer
854	FAB	21	Exploring Novel Via Fill and Planarization Technology	Reckert, Torsten	all4PCB	Circ

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855	ASSY	21	Manufacturing Optimization of Large BGAs Soldered on PCBs	Priore, Scott, etal	Cisco	SM
856	EMI	21	Electromagnetic Radiation and Human Health	Zamanian and Hard	Flour Corp	Higl
857	XMIS	21	Skewering Skew, Laminate Weave Induced Skew	Bogatin, Eric	Bogatin Ent	PC
858	FAB	21	Nonclassical Conductor Losses Due to Copper Foil Treatment	Brist, Gary etal	Intel	Circ
859	FAB	21	The State of Copper & Losses vs. Roughness	Hilburn, etal	Intel	PC
860	FAB	21	Impact of PCB Laminate Weave on Electrical Performance	McMorrow, Scott	Teraspeed	Des
861	FAB	21	Back Drilling to the Future	Ping, and Lingwen	Schenzen Ckts	Circ
862	TEST	21	Testing Serial Gigaherts-speed Buses	Schmitt, Alexander	Agilent	EDI
863	XMIS	21	Raytheon Memory Waveforms Showing Voltage Reversal		Raytheon	
864	FAB	21	Trace Etching and Undercuttin Picture		IPC	IPC
865	FAB	21	Test Procedure for New PCBs	Ritchey, Lee W	Speeding Edge	Spe
866	PS	21	Test Structure For PS Z vs F Testing	Ritchey, Lee W	Speeding Edge	Spe
867	FAB	21	PCB Surface Finishes	Ritchey, Lee W	Speeding Edge	Spe
868	CAP	21	Comparison of X2Y vs 0402 Capacitors for Decoupling	Zasio, John J	Caspian	Spe
869	XMIS	21	Test PCB Results for Procket High Speed Design	Ritchey, Lee W	Procket	Pro
870	FAB	21	Photo of Plating Steps, very good	?	PhotoCircuits	?
871	FAB	21	Diagram of Outer Layer Plating Steps		Multiwire	
872	FAB	21	Mahi Backplane A/W	Mahan, Victor	Mahi Networks	Mal
873	PS	21	RP2 Power Supply Measurements	Major, Don	Procket	Pro
874	DES	21	System Design Manual for Procket Networks	Ritchey, Lee W	Procket	Pro
875	XMIS	21	Magnuson Computer Test PCB	Ritchey, Lee W	Magnuson	Mag
876	DES	21	Straight Wire Inductance Chart	Moffat, Donald		Elec
877	SPEC	21	GR-78-CORE Dielectric Thickness Specs.			
878	SPEC	21	IPC-6012A Annular Ring Call out			IPC
879	SPEC	SHELF	IBIS Spec. Version 3.2 EIA0656-A	EIA	ANSI	ANS
880	SPEC	SHELF	GR-78-CORE Bellcore Telecom Product Requirements	Bell Comm	Bell Comm	Bell
881	SPEC	SHELF	Gr-1089-ILR EMC and Electrical Safety for TelCOM Products	Bellcore	Bell Comm	Bell
882	SPEC	SHELF	GR-63-CORE NEBS Requirements	Bellcore	Bell Comm	Bell
883	SPEC	BIN	Report on PCB Substrates- Good Picture of Plating Steps	Feeney, James	ADI/Isola	
884	SPEC	BIN	ADSPMM-88-308-BP High Speed Guidelines for USAF	Martin Marietta	Martin Marietta	Mar
885	SPEC	BIN	Voltage Drop Tests for Magnuson PCBs	Ritchey, Lee W	Magnuson	Mag
886	SPEC	BIN	Merix DFM Guide for Rigid PCBs		Merix	Mer
887	SPEC	BIN	ABCs of Probes	Tektronix		Tek
888	SPEC	BIN	STP DFM PCB Handbook	Rebmann etal	STP	STF
889	FAB	22	Alternative Surface Finish- Immersion Tin, Qual Report	Shpak, etal	Teradyne	Tera
890	FAB	22	Recognizing Intellingent Design- DFM issues	Ritchey, Lee W	Circuitree	Spe
891	ASSY	22	Assembly Issues with Microvia technologies (Good)			

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892	PS	22	Power Distribution System Design: Using Bypass/Decoupling Cap	Alexander, Mark	Xilinx	Xilir
893	MEM	**BIN**	512Mb M-die DDR2 SDRAM Specification Version 0.91		Samsung	San
894	PS	BIN	Measurement of Power-Distribution Networks and Their Elements	Novak, Istvan, etal	DesignCon03	SUI
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